CK COLLEGE OF ENGINEERING AND TECHNOLOGY
AN AUTONOMOUS INSTITUTION
CAVINKARE PATRONIZED INSTITUTION

C.K. COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution)

Approved by AICTE, Affiliated to Anna University & Recognized under UGC section 2(f) & 12(B)
Accredited by NAAC with 'A' grade and ISO 9001:2015 Certified Institution

Jayaram Nagar, Chellangkuppam, Cuddalore-607 003, Tamil Nadu, India.

DEPARTMENT OF
ME - APPLIED ELECTRONICS

CURRICULUM AND SYLLABI

I & II SEMESTER

(UNDER CKCET AUTONOMOUS REGULATION)

REGULATION 2026

Academic Year 2026-27 onwards

C. K. COLLEGE OF ENGINEERING AND TECHNOLOGY
(An Autonomous Institution)

POSTGRADUATE CURRICULUM

Department : Applied Electronics.

Programme : M.E. (Applied Electronics)

Regulations : 2026, with effect from the AY 2026 – 27 to all the students of Post Graduate Programme.

OVERVIEW OF CREDITS

Semester / Category	BS	ES (PC)	ES (PE)	OE	SD	SLC	RMC	Total
Semester – I	04	16	–	–	01	–	–	21
Semester – II	–	12	03	–	02	–	02	19
Semester – III	–	–	09	03	07	01	–	20
Semester – IV	–	–	–	–	12	–	–	12
Total Credits	**04**	**28**	**12**	**03**	**22**	**01**	**02**	**72**
Percentage (%)	**5.56**	**38.89**	**16.67**	**4.17**	**30.56**	**1.39**	**2.78**	**100**

CATEGORY OF COURSES

BS	Basic Science (Mathematics, Physics, Chemistry)	L	Laboratory
ES	Engineering Science	T	Theory
PC	Professional Core	LIT	Laboratory Integrated Theory
PE	Programme Elective	OE	Open Elective
SD	Skill Development	G	General
SLC	Self-Learning Course	MC	Mandatory Course
RMC	Research Methodology Course		

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Board of Studies of M.E (AE) Dept.
Meeting No.: 01 Dated: 28.3.26

Semester – I							
S. No.	Course Code	Course Name	Course Type	Periods/Week		Credits	Category
				L-T- P	TCP		
1.	26AE101T	Advanced Mathematical Methods	T	3-1-0	4	4	BS
2.	26AE102T	Statistical Signal Processing and Modeling	T	3-1-0	4	4	PC
3.	26AE103L	Advanced Digital System Design	LIT	3-0-2	5	4	PC
4.	26AE104T	Analog Integrated Circuit Design	T	3-0-0	3	3	PC
5.	26AE105T	Digital CMOS VLSI Design	T	3-0-0	3	3	PC
6.	26AE106P	Analog IC Design Laboratory	P	0-0-4	4	2	PC
7.	26AES01P	Technical Seminar	P	0-0-2	2	1	SD
Total Credits					**25**	**21**	

Semester – II							
S. No.	Course Code	Course Name	Course Type	Periods/Week		Credits	Category
				L-T- P	TCP		
1.	26AE201T	Industrial Internet of Things	T	3-1-0	4	4	PC
2.	26AE202T	High Speed Circuit Design	T	3-1-0	4	4	PC
3.	---	Programme Elective – I	T	3-0-0	3	3	PE
4.	26AE203L	Embedded System Design	LIT	3-0-2	5	4	PC
5.	---	Industry Oriented Course I	---	1-0-0	1	1	SD
6.	---	Industrial Training	---	---	---	1	SD
7.	26AE204T	Research Methodology and IPR	T	2-0-0	2	2	RMC
8.	---	Self-Learning Course – I	---	---	---	NC	MC
Total Credits					**19**	**19**	

Semester – III							
S. No.	Course Code	Course Name	Course Type	Periods/Week		Credits	Category
				L-T- P	TCP		
1.	---	Programme Elective – II	T	3-0-0	3	3	PE
2.	---	Programme Elective – III	T	3-0-0	3	3	PE
3.	---	Programme Elective – IV	T	3-0-0	3	3	PE
4.	---	Open Elective – I	T	3-0-0	3	3	OE

5.	---	Industry Oriented Course – II	T	1-0-0	1	1	SD
6.	---	Self – Learning Course – II	---	---	---	1	SLC
7.	26AE301P	Project Work I	P	0-0-12	12	6	SD
Total Credits					**25**	**20**	

Semester – IV							
S. No.	**Course Code**	**Course Name**	**Course Type**	**Periods/Week**		**Credits**	**Category**
				L-T- P	**TCP**		
1.	26AE401P	Project Work – II	P	0-0-24	24	12	SD
Total Credits					**24**	**12**	

Total Credits: 72

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PROGRAMME ELECTIVE (PE) COURSES

S. No	Course Code	Course Title	Periods per week			TCP	Credits
			L	T	P		
1	26AE001T	Digital Image and Video Processing	3	0	0	3	3
2	26AE002T	DSP Architecture and Programming	3	0	0	3	3
3	26AE003T	RF Integrated Circuit Design	3	0	0	3	3
4	26AE004T	Electromagnetic Interference and Compatibility	3	0	0	3	3
5	26AE005T	Advanced Microprocessor and Microcontroller Architectures	3	0	0	3	3
6	26AE006T	Advanced Computer Architecture Design	3	0	0	3	3
7	26AE007T	Signal Integrity for High-Speed Design	3	0	0	3	3
8	26AE008T	VLSI Interconnects	3	0	0	3	3
9	26AE009T	Semiconductor Memory Design	3	0	0	3	3
10	26AE010T	Algorithms for VLSI Physical Design Automation	3	0	0	3	3
11	26AE011T	Statistical Analysis and Optimization for VLSI	3	0	0	3	3
12	26AE012T	System on Chip Design	3	0	0	3	3
13	26AE013T	Hardware / Software Co-Design	3	0	0	3	3
14	26AE014T	MEMS and NEMS	3	0	0	3	3
15	26AE015T	Cryptography and Network Security	3	0	0	3	3
16	26AE016T	Neuromorphic Computing	3	0	0	3	3
17	26AE017T	Hardware Architecture for Artificial Intelligence	3	0	0	3	3
18	26AE018T	IP Core Design and Protection	3	0	0	3	3
19	26AE019T	Spintronics and Quantum Computing	3	0	0	3	3
20	26AE020T	Analog and Mixed Signal VLSI Design	3	0	0	3	3

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OPEN ELECTIVE (OE) COURSES

S. No	Course Code	Course Title	Periods per week			TCP	Credits
			L	T	P		
1	26AE901T	Electric Vehicle Technology	3	0	0	3	3
2	26AE902T	Micro and Small Business Management	3	0	0	3	3
3	26AE903T	Renewable Energy Technology	3	0	0	3	3
4	26AE904T	Design Thinking and User Experience	3	0	0	3	3
5	26AE905T	New Product Development	3	0	0	3	3

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Semester – I

26AE101T	Advanced Mathematical Methods	Category	L	T	P	C
		BS	3	1	0	4

Course Objectives:

- To introduce the concepts and applications of calculus of variations and direct optimization methods.
- To develop skills in queueing theory for analyzing and modeling service systems.
- To familiarize students with graph theory and graph algorithms for solving network problems.
- To impart knowledge of linear programming, transportation, and assignment optimization techniques.
- To develop competency in CPM and PERT for project planning, scheduling, cost control, and resource management.

Calculus of Variations

Variation and its properties, Euler's equation, Functionals dependent on first and higher order derivatives, Functionals dependent on functions of several independent variables, Some applications, Direct methods, Ritz method.

Queueing Models

Markovian queues, Birth and death processes, Single and multiple server queueing models, Little's formula, Queues with finite waiting rooms, Queues with impatient customers: Balking and reneging. Finite source models, M/G/1 queue, Pollaczek Khinchin formula, M/D/1 and M/EK/1 as special cases, Series queues, Open Jackson networks.

Graph Theory

Introduction to paths, trees, Isomorphism, Matrix coloring and directed graphs, Some basic algorithms: Dijkstra's Algorithm, Depth-First search, Breadth-First search, Prims Algorithm, Kruskal Algorithm.

Optimization Techniques - I

Linear Programming formulation, solution by graphical and simplex methods, Big M method, Transportation Models: (Minimising and Maximising Problems) – Balanced and unbalanced Problems – Initial Basic feasible solution by N-W Corner Rule, Least cost and Vogel's approximation methods. Check for optimality. Solution by MODI / Stepping Stone method. Assignment Models: (Minimising and Maximising Problems) – Balanced and Unbalanced Problems. Solution by Hungarian and Branch and Bound Algorithms.

Optimization Techniques - II

Project Management by CPM and PERT: Constructing project network, network computations in CPM and PERT, cost crashing, resource levelling.

Total periods (L: 45; T: 15): 60

Reference Books:

1. Elsgolc, L. D. – Calculus of Variations, Dover Publications.
2. Gross, D. & Harris, C. M. – Fundamentals of Queueing Theory, Wiley.
3. Deo, N.–Graph Theory with Applications to Engineering and Computer Science, PHI.
4. Hillier, F. S. & Lieberman, G. J –Introduction to Operations Research, McGraw-Hill.

5. Kanti Swarup, Gupta P.K., & Man Mohan–Operations Research, Sultan Chand & Sons.

E-resources:

1. https://nptel.ac.in/courses/111/105/111105039
2. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-262discrete-stochastic-processes
3. https://nptel.ac.in/courses/106/106/106106183

COURSE OUTCOMES:

At the end of the course, students will be able to:	
CO1	Apply the principles of calculus of variations to formulate and solve functional optimization problems.
CO2	Analyze and evaluate stochastic systems using queueing models and performance measures.
CO3	Apply graph theory concepts and algorithms to solve network-based problems.
CO4	Formulate and solve optimization problems using linear programming and operations research techniques.
CO5	Integrate advanced mathematical methods to analyze and solve complex constrained problems.

26AE102T	Statistical Signal Processing and Modeling	Category	L	T	P	C
		ES (PC)	3	1	0	4

Course Objectives:

- To understand random signal processing and statistical properties of signals.
- To develop signal models for prediction and estimation.
- To apply spectral estimation techniques.
- To design linear estimation filters using Wiener theory.
- To implement adaptive filtering algorithms for real-time applications.

Random Signal Processing

Review of discrete-time signals and systems, discrete random processes and ensemble averages, stationarity (strict & wide sense), autocorrelation and autocovariance functions, power spectral density (PSD), Wiener–Khintchine relation, Parseval's theorem, white noise and its properties, spectral factorization, linear filtering of random signals.

Signal Modeling and Prediction

Introduction to signal modeling, AR, MA, ARMA models, forward and backward linear prediction, Yule-Walker equations, Prony's method, Levinson-Durbin algorithm, model parameter estimation.

Spectral Estimation

Spectral estimation from finite-length signals, non-parametric methods: periodogram, Bartlett, Welch, Blackman-Tukey methods, parametric methods: AR spectral estimation, performance comparison, harmonic detection.

Linear Estimation and Wiener Filtering

Linear Minimum Mean Square Error (LMMSE) estimation, Wiener-Hopf equations, orthogonality principle, FIR and IIR Wiener filters, causal and non-causal filters, applications in noise cancellation and signal enhancement.

Adaptive Filters and Applications

Introduction to adaptive filtering, FIR adaptive filters, steepest descent algorithm, LMS, normalized LMS, RLS algorithms, convergence analysis, applications: adaptive equalization, echo cancellation, noise cancellation.

Total periods (L: 45; T: 15): 60

Reference Books:

1. M. H. Hayes, Statistical Digital Signal Processing and Modeling, John Wiley & Sons, 2002.
2. D. G. Manolakis and V. K. Ingle, Applied Digital Signal Processing, Cambridge University Press, 2011.
3. S. M. Kay, Fundamentals of Statistical Signal Processing: Estimation Theory, Prentice Hall, 2017.
4. T. Kailath, A. H. Sayed, and B. Hassibi, Linear Estimation, Prentice Hall, 2000.
5. J. G. Proakis and D. G. Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, Pearson, 2013.

COURSE OUTCOMES:

At the end of the course, students will be able to:	
CO1	Describe random processes and their statistical properties such as stationarity, autocorrelation, and power spectral density
CO2	Analyze and model signals using AR, MA, and ARMA techniques for prediction and estimation.
CO3	Apply parametric and non-parametric spectral estimation methods for frequency domain analysis.
CO4	Design linear estimation filters using Wiener theory for signal enhancement and noise reduction.
CO5	Implement adaptive filtering algorithms for real-time signal processing applications.

26AE103L	Advanced Digital System Design	Category	L	T	P	C
		ES (PC)	3	0	2	4

Course Objectives:

- To study the design and analysis of synchronous and asynchronous sequential circuits.
- To understand PLD and ROM-based digital system design.
- To learn testing techniques for combinational circuits and PLA.
- To develop digital systems using Verilog HDL.

Sequential Circuit Design

State diagrams/tables, state assignment & reduction, synchronous circuit design, iterative circuits, ASM charts.

Activities

1. Design state diagrams and state tables for given problem.
2. Design and analyze synchronous sequential circuits using ASM charts.

Asynchronous Sequential Circuit Design

Flow table reduction, race conditions, hazards (static/dynamic/essential), mixed-mode circuits, vending machine controller design.

Activities

3. Construct and minimize flow tables for asynchronous circuits.
4. Identify race conditions and hazards in given circuits.

Fault Diagnosis and Testability Algorithms

Fault table, path sensitization, Boolean difference, D & Kohavi algorithms, PLA faults, DFT, BIST techniques.

Activities

5. Generate fault tables for combinational circuits.
6. Apply D-algorithm for fault detection.

Synchronous Design Using Programmable Devices

PLD families, PLA/PAL-based circuit design, ROM design, FSM realization using PLDs, FPGA (Xilinx Vertex 7).

Activities

7. Design digital circuits using PLA/PAL.
8. Implement FSM using programmable logic devices.

System Design Using Verilog

Verilog HDL modeling, data types, behavioral & structural modeling, FSM synthesis, test benches, combinational/sequential circuit realization.

Activities

9. Write and simulate Verilog code for basic digital circuits.
10. Design and verify FSM using Verilog HDL.

Practical Exercises:

1. Design and implementation of synchronous sequential circuits using state diagrams and ASM charts.
2. Design and analysis of asynchronous sequential circuits using flow tables.
3. Identification and elimination of race conditions and hazards in asynchronous circuits.
4. Generation of fault tables and fault detection using D-algorithm.
5. Design and implementation of digital circuits using PLA/PAL and ROM.
6. Implementation of Finite State Machines (FSM) using programmable logic devices / FPGA.
7. Modeling and simulation of combinational circuits using Verilog HDL.
8. Design and simulation of sequential circuits (flip-flops, counters, registers) using Verilog.
9. Design and verification of FSM using Verilog HDL and test benches.
10. Design and implementation of a simple digital system using Verilog HDL.

Total periods (L: 45; P: 30): 75

COURSE OUTCOMES:

At the end of the course, students will be able to:	
CO1	Explain the fundamentals of synchronous and asynchronous sequential circuits.
CO2	Analyze sequential circuits using state diagrams and ASM charts.
CO3	Design sequential circuits using state diagrams and ASM charts.
CO4	Apply fault diagnosis and testability algorithms to digital circuits.
CO5	Develop and simulate digital systems using Verilog HDL and FPGA.

26AE104T	Analog Integrated Circuit Design	Category	L	T	P	C
		ES (PC)	3	0	0	3

Course Objectives:

- To study single-stage amplifier design and analysis.
- To understand high-frequency response and noise characteristics of amplifiers.
- To analyze operational amplifier circuits and applications.
- To design voltage and current reference circuits.

Single Stage Amplifiers

MOS physics, equivalent circuits, CS, CG, source follower, differential & cascode amplifiers, design for SR, gain, BW, ICMR, power, voltage swing.

High Frequency and Noise Characteristics of Amplifiers

Miller effect, pole analysis, frequency response of stages, noise sources, noise analysis in single stage and differential amplifiers.

Negative Feedback Amplifiers and Operational Amplifiers

Feedback types, loading effects, op-amp parameters, one/two-stage op-amps, gain boosting, slew rate, PSRR, noise in op-amps.

Stability and Frequency Compensation of Two Stage Operational Amplifier

Two stage op-amp analysis, phase margin, compensation methods, slew rate issues, advanced compensation techniques.

Voltage and Current References

Current mirrors (Wilson, Widlar, Cascode), high swing cascode sinks, supply/temperature independent biasing, PTAT & CTAT currents, constant-Gm biasing.

Total periods: 45

Reference Books:

1. References: 1. Allen, P. E., & Holberg, D. R. (2013). CMOS analog circuit design (3rd ed.). Oxford University Press.
2. Baker, R. J. (2019). CMOS: Circuit design, layout, and simulation (4th ed.). Wiley IEEE Press.
3. Grebene, A. B. (2003). Bipolar and MOS analog integrated circuit design. John Wiley & Sons.
4. Natarajan, A. (n.d.). EE5390: Analog IC design [Recorded lecture]. http://www.ee.iitm.ac.in/~ani/ee5390/index.html
5. Razavi, B. (2016). Design of analog CMOS integrated circuits (2nd ed.). Tata McGraw Hill.
6. Sansen, W. M. C. (2007). Analog design essentials. Springer.

COURSE OUTCOMES:

At the end of the course, students will be able to:	
CO1	Explain the theory and design concepts of analog circuits.
CO2	Analyze single-stage amplifiers considering high-frequency and noise characteristics.

CO3	Design multi-stage amplifiers to meet specified performance criteria.
CO4	Apply concepts of negative feedback, stability, and frequency compensation in operational amplifier design.
CO5	Design voltage and current reference circuits with temperature and supply independence.

26AE105T	Digital CMOS VLSI Design	Category	L	T	P	C
		ES (PC)	3	0	0	3

Course Objectives:

- To understand CMOS fundamentals and circuit operation.
- To design combinational and sequential CMOS circuits.
- To apply structured VLSI design methodologies.
- To analyze digital systems through case studies.

MOS Transistors and CMOS Inverter

MOS transistor characteristics, short channel effects, CMOS inverter design, stick diagrams, power, delay, sizing.

CMOS, Combinational Circuits

Complementary CMOS, power reduction, ratioed logic, pass transistor logic, dynamic CMOS, Domino, NP-CMOS.

CMOS, Sequential Circuits

Latches vs registers, flip-flops, dynamic/static registers, clocking strategies, Schmitt trigger, mono/astable circuits.

CMOS Sub System Design

Adders (carry bypass, select, CLA), multipliers, counters, parity generators, multiplexers, shifters, memory elements.

Performance Estimation & Design Techniques

Delay estimation, logical effort, sizing, power, interconnects, scaling, synchronous and self-timed design.

Total periods: 45

Reference Books:

1. Weste, N. H. E., & Harris, D. (2011). CMOS VLSI design: A circuits and systems perspective. Pearson.
2. Rabaey, J. M., Chandrakasan, A., & Nikolić, B. (2003). Digital integrated circuits. Pearson.
3. Martin, K. (2011). Digital integrated circuit design. Oxford University Press.
4. Palnitkar, S. (2003). Verilog HDL (2nd ed.). Pearson Education.

COURSE OUTCOMES:

At the end of the course, students will be able to:	
CO1	Explain CMOS fundamentals in digital circuits.
CO2	Analyze CMOS-based combinational circuits.
CO3	Design CMOS-based sequential circuits.
CO4	Apply CMOS logic styles and techniques for optimizing digital subsystems.
CO5	Evaluate circuit performance using structured VLSI design approaches.

26AE106P	Analog IC Design Laboratory	Category	L	T	P	C
		ES (PC)	0	0	4	2

Course Objectives:

- To Design analog circuits from transistor level to IA implementation using CAD tools for simulation, layout, LVS, and parasitic extraction.

List of Experiments

1. **Extraction of process parameters of CMOS process transistors**
   a. Plot I_D vs V_{GS} and determine threshold voltage V_t.
   b. Plot $\log I_D$ vs V_{GS} to obtain I_{OFF} and subthreshold slope.
   c. Plot I_D vs V_{DS} for different V_{GS} to find channel length modulation.
   d. Extract parameters using SPICE: g_m, g_{ds}, and V_t.
   e. Tabulate and compare results for NMOS and PMOS.
2. **CMOS inverter design and performance analysis**
   a. Plot VTC of CMOS inverter and determine transition voltage, gain, V_{IL}, V_{IH}, NMH, and NML.
   b. Plot VTC for different V_{DD} values and device ratios.
   c. Perform transient analysis (with and without load) to find t_{pHL}, t_{pLH}, rise time (t_r), and fall time (t_f).
   d. Perform AC analysis for fanout 0 and fanout 1.
3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.
4. **Single stage amplifier design and performance analysis**
   a. Plot small-signal voltage gain of a CMOS inverter versus input DC voltage and determine gain at switching point; compare for two technologies.
   b. Design a common-source (CS) amplifier with NMOS driver and PMOS active load.
   c. Establish test bench with $V_{DSQ} = V_{DD}/2$; calculate input bias voltage and bias current.
   d. Perform SPICE simulation and compare theoretical and simulated bias current.
   e. Determine voltage gain, -3 dB bandwidth, and gain-bandwidth product (GBW).
   f. Plot step response, find time constant, and compare with -3 dB bandwidth.
   g. Determine input voltage range of the amplifier.
5. **Three OPAMP Instrumentation Amplifier (INA).**
   a. Design a three-op-amp INA with overall gain = 10 (stage gains: 2 and 5).
   b. Draw schematics of the op-amp macro model and INA.
   c. Determine op-amp parameters: low-frequency gain, unity gain bandwidth, input capacitance, output resistance, and CMRR.
   d. Set up CMRR simulation and perform AC analysis of INA; compare with op-amp CMRR.
   e. Analyze effect of resistor mismatch (−5% to +5%) on INA CMRR and plot results.
   f. Repeat analysis for different op-amp gain settings and compare performance.
6. **Use Layout editor.**
   a. Draw layout of a minimum-size CMOS inverter using Metal 1 interconnect.
   b. Perform DRC, LVS, and RC extraction; ensure no errors.
   c. Extract netlist and determine t_{PHL} and t_{PLH} using SPICE.
   d. Connect three inverters in a chain with specified interconnect length.

e. Extract new netlist and measure delay of the middle inverter.
f. Compare delay values with initial results.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter a. low-frequency voltage gain, b. unity gain BW (fu), c. Power dissipation

a. Determine low-frequency gain, unity gain bandwidth (f_u), and power dissipation.
b. Perform DC analysis to find input common-mode range and compare with theoretical values.
c. Perform time-domain simulation to verify low-frequency gain.
d. Perform AC analysis to verify frequency response.

Total periods: 60

Reference Books:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.
2. Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, 2012.
3. David A. Johns and Ken Martin, Analog Integrated Circuit Design, Wiley, 1997.
4. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, Wiley, 2010.
5. R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, Wiley-IEEE Press, 2019.
6. Geiger, Allen, and Strader, VLSI Design Techniques for Analog and Digital Circuits, McGraw-Hill, 1990.
7. Cadence Design Systems, Virtuoso User Guide and Documentation.

COURSE OUTCOMES:

At the end of the course, students will be able to:	
CO1	Characterize MOS transistors using simulation tools.
CO2	Design basic analog building blocks using simulation tools.
CO3	Implement and simulate analog circuits using schematic entry.
CO4	Perform layout design, LVS, and parasitic extraction.
CO5	Design and validate an instrumentation amplifier using CAD tools.

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Semester – II

26AE201T	Industrial Internet of Things	Category	L	T	P	C
		ES (PC)	3	1	0	4

Course Objectives:

- To understand IoT nodes and sensor technologies.
- To study IoT gateways and communication protocols.
- To explore IoT cloud systems and data management.
- To develop IoT cloud dashboards for visualization.
- To analyze challenges in IoT system design.

Understanding IOT Concept and Development Platform

IOT Definition, Importance of IoT, Applications of IOT, IoT architecture, Understanding working of Sensors, Actuators, Sensor calibration, Study of Different sensors and their characteristics.

Analysing & Decoding of Communication Protocol Used in IOT Development Platform

UART Communication Protocol, I2C Protocol device interfacing and decoding of signal, SPI Protocol device interfacing and decoding of signal, WIFI and Router interfacing, Ethernet Configuration, Bluetooth study and analysis of data flow, Zigbee Interfacing and study of signal flow.

IOT Physical Devices and Endpoints and Controlling Hardware and Sensors

IoT Physical Devices and Endpoints- Introduction to Arduino and Raspberry Pi- Installation, Interfaces (serial, SPI, I2C), Programming – Python program with Raspberry PI with focus on interfacing external gadgets, controlling output, reading input from pins. Controlling Hardware- Connecting LED, Buzzer, Switching High Power devices with transistors, Controlling AC Power devices with Relays, Controlling servo motor, speed control of DC Motor, unipolar and bipolar Stepper motors; Sensors- Light sensor, temperature sensor with thermistor, voltage sensor, ADC and DAC, Temperature and Humidity Sensor DHT11, Motion Detection Sensors, Wireless Bluetooth Sensors, Level Sensors, USB Sensors, Embedded Sensors, Distance Measurement with ultrasound sensor.

Cloud Services Used in IOT Development Platform

Configuration of the cloud platform, Sending data from the IOT nodes to the gateways using different communication options; Transferring data from gateway to the cloud; Exploring the web services like mail, Messaging (SMS) and Twitter etc.; Tracking of cloud data as per the requirement; Google Cloud service architect; AWS cloud Services architect; Microsoft Azure cloud services Architect; Open-source Cloud Services; Initial State IoT Dashboard & Cloud Services.

Challenges in IOT System Design – Hardware & Software

Antenna design and placement, Chip-package system development, Power electronics, electromagnetic interference/compatibility (EMI/EMC), Electronics reliability; Battery simulation.

Total periods (L: 45; T: 15): 60

Reference Books:

1. Bahga, A., & Madisetti, V. (2015). Internet of things: A hands-on approach. Universities Press. https://doi.org/9788173719547.

2. Richardson, M., & Wallace, S. (2014). Getting started with Raspberry Pi. O'Reilly (SPD). https://doi.org/9789350239759.
3. Monk, S. (2016). Raspberry Pi cookbook: Software and hardware problems and solutions. O'Reilly (SPD). https://doi.org/9789352133895.
4. Ida, N. (2014). Sensors, actuators and their interfaces. SciTech Publishers.
5. Waher, P. (2015). Learning Internet of Things. Packt Publishing.

COURSE OUTCOMES:

At the end of the course, students will be able to:	
CO1	Understand IoT concepts, architecture, sensors, actuators, and development platforms.
CO2	Analyze and decode communication protocols like UART, I2C, SPI, WiFi, Bluetooth, and Zigbee.
CO3	Interface and control IoT physical devices, sensors, and actuators using platforms like Arduino and Raspberry Pi.
CO4	Use cloud platforms for IoT data management, dashboard creation, and real-time monitoring.
CO5	Identify and address hardware and software challenges in IoT system design, including EMI/EMC and power considerations.

26AE202T	High Speed Circuit Design	Category	L	T	P	C
		ES (PC)	3	1	0	4

Course Objectives:

- To introduce the fundamentals of PCB design.
- To understand high-speed PCB design techniques.
- To analyze signal integrity issues in PCB design.
- To develop PCB layouts using CAD tools.
- To gain hands-on experience in PCB design and fabrication.

PCB Basics, Fabrication and Standards

Printed Circuit Board fabrication, PCB cores and layer stack-up, fabrication processes (photolithography, chemical etching, mechanical milling, layer registration), role of layout in PCB design, design files (layout files, Gerber files, assembly layers), standards organizations, PCB classes and types, fabrication allowances, PCB dimensions and tolerances, copper trace tolerances, hole dimensions, soldermask tolerances.

PCB Design Flow using CAD Tools

Overview of CAD tools, project setup, schematic entry, component placement and wiring, schematic-to-layout conversion, layout environment, routing techniques (manual and auto), design rule check, board outline creation, post-processing for manufacturing, Gerber file generation, fabrication submission, inspection and testing, nonstandard Gerber files.

Design for Manufacturability (DFM)

PCB assembly and soldering processes, component placement and orientation, spacing rules for THD and SMD, mixed THD and SMD design considerations, footprint and pad stack design, land patterns for SMD and THD, hole-to-lead ratio, annular ring width, clearance issues, solder mask and solder paste design.

High Speed PCB Design and Signal Integrity

Introduction to high-speed PCB design, signal integrity concepts, causes of signal integrity issues, PCB transmission lines, controlled impedance, electromagnetic compatibility (EMC), power integrity.

PCB Stackup and High-Speed Technology

PCB stackup design, stackup terminology, selection of high-speed materials, effect of fiberglass weave on impedance characteristics.

Total periods (L: 45; T: 15): 60

Text Books:

1. Mitzner, K. (2009). Complete PCB design using OrCAD Capture and Layout (1st ed.). Newnes.
2. Monk, S. (2017). Make your own PCBs with EAGLE: From schematic design to finished boards (2nd ed.). McGraw-Hill Education TAB.
3. Sierra Circuits Inc. (2020). High-speed PCB design guide.
4. Brooks, D. (2012). Signal integrity issues and printed circuit board design. Prentice Hall PTR.

5. Ritchey, L. W., Zasio, J., & Knack, K. J. (2003). Right the first time: A practical handbook on high-speed PCB and system design. Speeding Edge.
6. COEP Virtual Labs. (n.d.). PCB design and fabrication.

E - Resources:

1. https://fab-coep.vlabs.ac.in/exp/pcb-design-fabrication/.
2. NPTEL. (n.d.). PCB design online course. https://onlinecourses.nptel.ac.in/noc24_ee127/preview.

COURSE OUTCOMES:

At the end of the course, students will be able to:	
CO1	Understand the basics of PCB design, fabrication, layers, standards, tolerances, and design files.
CO2	Apply CAD tools for PCB design, schematic entry, layout creation, auto/manual routing, and DRC.
CO3	Design PCB considering manufacturability constraints including component spacing, padstack, and soldermask.
CO4	Analyze high-speed PCB design considerations including signal integrity, EMC/EMI, transmission lines, and power integrity.
CO5	Design and optimize high-speed PCB stackups and select suitable materials and routing strategies for signal-integrity requirements.

26AE203L	Embedded System Design	Category	L	T	P	C
		ES (PC)	3	0	2	4

Course Objectives:

- To understand embedded computing system design including hardware and software.
- To analyze distributed embedded architectures and communication protocols.
- To study ARM processor architecture and programming.
- To design embedded systems using hardware-software co-design.
- To implement real-time embedded applications.

Embedded Computing Platform

Embedded computers, characteristics of embedded applications, challenges in embedded system design, embedded system design process, CPU fundamentals (programming, I/O operations), CPU performance and power consumption, CPU buses, memory devices, input/output devices, component interfacing, microprocessor-based system development and debugging.

Activities:

1. Microprocessor I/O Interfacing.
2. CPU Performance and Power Measurement.

Distributed Embedded Systems

Multiprocessors, CPUs and accelerators, performance analysis, distributed embedded architecture, communication networks for embedded systems (I2C, CAN, SHARC link port, Ethernet, Myrinet), network-based design, Internet-enabled systems, system-level performance analysis.

Activities:

3. Network Communication in Embedded Systems.
4. Multiprocessor Performance Analysis.

ARM Processor and Programming

ARM processor fundamentals, ARM Cortex-M3 architecture, MBED NXP LPC1768, pin configuration and peripherals, ARM instruction set, addressing modes, ARM assembly language programming.

Activities:

5. ARM Cortex-M3 Architecture Exploration.
6. ARM Assembly Programming.

Embedded System Design and Case Studies

Design models, system architecture, hardware and software co-design, quality assurance, design examples: toy train controller, digital alarm clock, telephone PBX, inkjet printer, personal digital assistants, set-top box.

Activities:

7. Embedded System Case Study.
8. Hardware-Software Co-Design Exercise.

Embedded Applications and Implementation

Interfacing of sensors, displays, motors, communication protocols (I2C, SPI, CAN, UART), embedded system implementation techniques, robotic and real-time applications.

Activities:

9. Sensor, actuator, and communication interfacing
10. Embedded system project implementation

Total periods (L :45; P:30): 75

Practical Exercises:

1. Push button, LED, LCD display and RTC interfacing with AVR RISC based microcontroller.
2. AVR RISC based Microcontroller system design with Touch screen interfacing.
3. Motor (DC, stepper, servo) interfacing with AVR RISC based Microcontroller.
4. Interfacing sensors and RFID with AVR RISC based Microcontroller.
5. Design of RC5 remote control decoder with AVR RISC based Microcontroller.
6. Implementing I2C, SPI, CAN and UART protocols with ARM 7 processor.
7. Design and implementation of path tracking and obstacle avoidance Robot.
8. Design and implementation of self-balancing Robot.
9. Design and implementation of Robotic Arm manipulation with 6 DOF.
10. Design and implementation of Pick and Place robot.
11. Design and implementation of color and pattern guided material handling robot.
12. Design and implementation of human detection robot using PIR sensor.

Reference Books:

1. Wolf, W. (2012). Computers as components: Principles of embedded computing system design (3rd ed.), Morgan Kaufmann Publishers.
2. Sloss, A. N., Symes, D., & Wright, C. (2008). ARM system developer's guide: Designing and optimizing system software. Elsevier/Morgan Kaufmann.
3. Elahi, A., & Arjeski, T. (2015). ARM assembly language with hardware experiments. Springer.
4. Liu, J. W. S. (2001). Real-time systems. Pearson Education Asia.
5. Krishna, C. M., & Shin, K. G. (2017). Real-time systems (1st ed., reprint). McGraw-Hill.
6. Vahid, F., & Givargis, T. (2006). Embedded system design: A unified hardware/software introduction. John Wiley & Sons.

COURSE OUTCOMES:

At the end of the course, students will be able to:	
CO1	Explain the design, development, and optimization of embedded computing platforms including CPU, memory, buses, and I/O devices.
CO2	Apply distributed embedded computing concepts, multiprocessor architectures, and communication protocols (I2C, CAN, Ethernet).
CO3	Analyze ARM processor architecture, instruction set, and peripherals.
CO4	Design embedded system applications using hardware-software co-design approaches and case studies.
CO5	Implement embedded system projects involving sensors, actuators, communication protocols, and robotic systems.

26AE204T	Research Methodology and IPR	Category	L	T	P	C
		RMC	2	0	0	2

Course Objectives:

- To understand the fundamentals of research design and research methodologies.
- To learn data collection methods, measurement techniques, and sampling strategies.
- To analyze data using statistical and multivariate techniques.
- To develop skills in interpreting and presenting research findings.
- To understand the concepts, types, and legal aspects of Intellectual Property Rights (IPR) and patents.

Research Design

Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.

Data Collection and Sources

Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.

Data Analysis and Reporting

Overview of Multivariate analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation.

Intellectual Property Rights

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Biodiversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

Patents

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.

Total periods: 30

Reference Books:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education, 11e (2012).
2. Catherine J. Holland, “Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets”, Entrepreneur Press, 2007.
3. David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007.
4. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.

COURSE OUTCOMES:

At the end of the course, students will be able to:	
CO1	Explain the principles of research design and select appropriate qualitative, quantitative, exploratory, survey, observational, and experimental methods for addressing research questions.
CO2	Apply appropriate measurement scales, questionnaires, instruments, and sampling techniques to collect reliable and relevant research data.
CO3	Analyze research data using appropriate hypothesis testing, measures of association, and multivariate analysis techniques and communicate findings through effective reports and presentations.
CO4	Explain the concepts, types, features, and practices of Intellectual Property Rights and identify their relevance to innovation, biodiversity, and technology development.
CO5	Apply the principles and procedures of patenting to evaluate inventions and understand patent filing, examination, grant, licensing, assignment, and related processes.

Approved by
Academic Council Meeting
No.: 01 Dated: 21.4.26

Recommended by
Board of Studies of M.E (AE) Dept.
Meeting No.: 01 Dated: 28.3.26

Programme Elective Courses

26AE001T	Digital Image and Video Processing	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand advanced concepts in digital image and video processing.
- To analyze temporal information and motion in video sequences.
- To apply techniques for motion estimation, tracking, and 3D reconstruction.
- To study video compression and deep learning-based analysis methods.
- To design and implement image and video processing systems for real-world applications.

Motion Estimation and Video Fundamentals

Temporal vs. spatial image processing - Basics of video formation and representation (color video, interlaced vs. progressive) - Frame differencing and background subtraction - Block matching algorithms (Full Search, Three Step Search, Diamond Search) - Optical flow (Lucas-Kanade and Horn-Schunck methods) - Applications: surveillance, object tracking.

Activity 1:

Motion Estimation with OpenCV (Block Matching vs. Optical Flow) - Tools: OpenCV (Python), sample videos (e.g., from UCF101 dataset) - Task: Implement and compare block matching and optical flow algorithms (Lucas-Kanade & Farnebäck) on test videos. - Outcome: Analyze tracking performance under different motion types.

Activity 2:

Flipped Class + Mini Project on Background Subtraction Techniques - Tools: OpenCV, Code samples from GitHub - Task: Pre-class video lectures + in-class implementation of MOG2 and KNN background subtraction on surveillance footage. - Outcome: Comparative report and demonstration of real-time performance.

Video Compression Standards and Techniques

Temporal redundancy and inter-frame coding - Overview of video compression standards: MPEG-1/2/4, H.264/AVC, HEVC - Intra vs. inter coding, GOP structure - Motion compensation and entropy coding in video codecs - Scalable and Multiview video coding.

Activity 1:

Video Codec Analysis using FFmpeg - Tools: FFmpeg (open source), sample videos from Xiph.org Video Test Media - Task: Encode videos using H.264, MPEG-4, and HEVC. Evaluate size, PSNR, and SSIM. - Outcome: Compression efficiency report.

Activity 2:

Flipped Classroom on GOP Structure - Tools: Handbrake + OpenCV + Python - Task: Analyze Group of Pictures (GOP) in compressed video streams. - Outcome: Presentation on impact of GOP length and I/P/B frame configuration.

3D Image Processing and Multiview Video

Stereoscopic imaging and disparity map estimation - 3D reconstruction from multiple images - Structure from motion (SfM) - Multiview video systems and depth estimation - Applications in VR/AR and 3D television.

Activity 1:

Stereo Vision and Disparity Map Generation - Tools: OpenCV stereo block matching, Middlebury Stereo Dataset - Task: Compute disparity maps from stereo pairs and visualize depth. - Outcome: Depth map quality evaluation and report.

Activity 2:

Structure from Motion (SfM) using COLMAP - Tools: COLMAP (open source SfM), ETH3D dataset - Task: Reconstruct sparse and dense 3D scenes from multiple views. - Outcome: 3D point cloud visualization and reconstruction accuracy analysis.

Advanced Image and Video Analysis

Video segmentation and object tracking (Kalman filter, mean-shift, particle filter) - Action and gesture recognition - Scene understanding and semantic segmentation - Face and emotion recognition in video - Deep learning applications: CNNs for video, 3D CNNs, RNNs/LSTMs.

Activity 1:

Action Recognition using Pre-trained CNN-LSTM Models Tools: PyTorch or TensorFlow, UCF101 dataset - Task: Use pretrained 3D CNN + LSTM pipeline to classify video actions. - Outcome: Confusion matrix + model performance summary.

Activity 2:

Seminar on Research Paper Reproduction - Task: Reproduce a recent CVPR/ICCV paper (e.g., Deep SORT, YOLOv7 tracking) using open-source codebases. - Outcome: Present implementation steps, results, and challenges faced.

Real-Time Processing and Applications

Real-time image/video processing architectures (GPU, FPGA) - Edge AI and deployment on embedded devices - High-speed video capture and analysis - Applications: autonomous driving, medical video analysis, drone surveillance - Case studies and open research challenges.

Activity 1:

Real-Time Object Tracking using Jetson Nano / Raspberry Pi - Tools: OpenCV + YOLOv5 or MobileNet-SSD, webcam or real-world video - Task: Deploy real time object tracker on edge device. - Outcome: Demonstrate live tracking with FPS metrics.

Activity 2:

Industry Case Study + Application Prototype - Task: Case study discussion on a real-world use (e.g., medical video analysis or drone surveillance) + student prototype. - Tools: Custom project using open-source libraries (e.g., OpenMMLab) - Outcome: Presentation + demo + report.

Total periods: 45

Reference Books:

1. Szeliski, R. (2022). Computer vision: Algorithms and applications (2nd ed.). Springer.
2. Bovik, A. C. (Ed.). (2020). The essential guide to video processing (2nd ed.). Academic Press.
3. Singh, R. (2023). Digital image and video processing: Principles and algorithms (1st ed.). McGraw-Hill Education.
4. Marques, O. (2019). Practical image and video processing using MATLAB (2nd ed.). Wiley.
5. Goodfellow, I., Bengio, Y., & Courville, A. (2021). Deep learning (2nd ed.). MIT Press.

E-Resources

1. NPTEL Course: Digital Image Processing by Prof. P.K. Biswas, IIT Kharagpur.
2. NPTEL Course: Computer Vision by Prof. S. Raman, IIT Gandhinagar.
3. OpenCV Tutorials: https://docs.opencv.org/4.x/d6/d00/tutorial_py_root.html.
4. Coursera Course: Applied Computer Vision with Deep Learning (DeepLearning.AI).
5. CMU Video Lectures: Computer Vision (16-720) on YouTube.

26AE002T	DSP Architecture and Programming	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand the fundamentals of Digital Signal Processors (DSPs).
- To study DSP architectures and their features.
- To develop programming skills for DSP processors.
- To analyze advanced DSP architectures.
- To explore applications of DSP in real-world systems.

Fundamentals of Programmable DSPs

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

TMS320C5X Processor

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

TMS320C6X Processor

Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction – DSP Starter Kit Support Tools- Code Composer Studio - Support Files - Programming Examples to Test the DSK Tools – Application Programs for processing real time signals.

ADSP Processors

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

Advanced Processors

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

Total periods: 45

Reference Books:

1. Singh, A., & Srinivasan, S. (2012). Digital signal processing: Implementations using DSP microprocessors with examples from TMS320C54xx. Cengage Learning India Private Limited.
2. Venkataramani, B., & Bhaskar, M. (2003). Digital signal processors: Architecture, programming and applications. Tata McGraw-Hill Publishing Company Limited.
3. Chassaing, R. (2005). Digital signal processing and applications with the C6713 and C6416 DSK. John Wiley & Sons.
4. Texas Instruments, Analog Devices, & Motorola. (n.d.). User guides.

26AE003T	RF Integrated Circuit Design	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To study CMOS transceiver architectures for communication systems.
- To analyze noise and impedance matching in RF circuits.
- To design amplifiers and feedback systems.
- To understand the operation of mixers and oscillators.
- To develop frequency synthesizers for high-performance communication systems.

CMOS Physics, Transceiver Specifications and Architectures

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct up conversion Transmitter, Two step up conversion Transmitter.

Activity:

Analysis of CMOS Transceiver Architectures and Noise Performance in Communication Systems.

Impedance Matching and Amplifiers

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

Activity:

Design and Analyze a Source-Degenerated Common-Source LNA Using S Parameters and Smith Chart–Based Impedance Matching.

Feedback Systems and Power Amplifiers

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.

Activity:

Analyze Stability, Efficiency, and Linearity in Class A–F Power Amplifiers Using Gain/Phase Margin, Root-Locus, and ACPR Evaluation.

Mixers and Oscillators

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

Activity:

Analyze and Compare Mixer Architectures and Oscillator Designs Using Nonlinear Characteristics, Describing Functions, and Phase-Noise Evaluation.

PLL and Frequency Synthesizers

Linearized Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

Activity:

Model and Evaluate a PLL-Based Integer-N Frequency Synthesizer Using Linearized Loop Analysis, Noise Characterization, and Phase-Detector/Charge-Pump Design.

Total periods: 45

Reference Books:

1. Lee, T. (2004). Design of CMOS RF integrated circuits. Cambridge University Press.
2. Razavi, B. (2013). RF microelectronics (2nd ed.). Pearson Education.
3. Crols, J., & Steyaert, M. (1997). CMOS wireless transceiver design. Kluwer Academic
4. Publishers.
5. Razavi, B. (2017). Design of analog CMOS integrated circuits (2nd ed.). McGraw-Hill
6. Education.
7. Indian Institute of Technology Madras. (n.d.). EE6240 – Recorded lectures and notes.
8. http://www.ee.iitm.ac.in/~ani/ee6240/.

26AE004T	Electromagnetic Interference and Compatibility	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand the fundamentals of EMI and EMC in electronic systems.
- To identify EMI sources and coupling mechanisms.
- To apply mitigation techniques such as shielding, grounding, and filtering.
- To study national and international EMC standards and regulations.
- To gain knowledge of EMI/EMC testing methods and instrumentation.
- To design electromagnetically compatible electronic systems and PCBs.

Introduction to EMI & EMC

Definitions and Concepts – EMC Environment - EMC Testing Categories - Basic Electromagnetic Theory: Maxwell's equations and their application in EMC, Near-field and far-field approximations, Concepts of impedance.

Activity 1: EMI Source Identification & Classification.
Activity 2: Near-Field vs Far-Field Exploration Using Simple Calculations.

EMI Coupling Mechanisms

Coupling Paths - basic coupling mechanisms: Conducted Coupling, Capacitive Coupling, Inductive/Magnetic Coupling, Radiative / Electromagnetic Coupling – Crosstalk - Transient Sources - Automotive transients.

Activity 1: Identify and Classify EMI Coupling Mechanisms in Real Devices.
Activity 2: Hands-On Demonstration of Crosstalk and Transient Effects.

EMI Mitigation Techniques & EMC Standards

Shielding – Grounding – Filtering – Cabling – Bonding - Need for Standards - National and International EMC Standardizing Organizations: IEC, FCC, CISPR, ANSI, BSI, CENELEC, ETSI - Key Standards and Specifications: MIL-STD, Electro Magnetic Emission and Susceptibility standards.

Activity 1: EMI Mitigation Hands-On Experiment.
Activity 2: EMC Standards Research & Presentation.

EMI Test Methods and Instrumentation

Fundamental Considerations - Emission Testing: Conducted Emissions, Radiated Emissions - Immunity/Susceptibility Testing: Conducted Immunity, Radiated Immunity, ESD Testing, Transient Immunity - Test Equipment.

Activity 1: Emission Testing Demonstration
Activity 2: Immunity and ESD Testing Simulation

PCB Design for EMC Compliance

PCB Layout and Stack-up - Signal Integrity Considerations - Mixed-Signal PCB Layout: Grounding and power distribution for mixed-signal systems, Isolation of sensitive circuits - Component Placement for EMC.

Activity 1: Analyzing PCB Layout for EMC Issues.
Activity 2: Design a Simple EMC-Compliant PCB Section.

Total periods: 45

Reference Books:

1. Ott, H. W. (1988). Electromagnetic compatibility engineering (2nd ed.). John Wiley & Sons.
2. Paul, C. R. (2010). Introduction to electromagnetic compatibility (2nd ed.). Wiley Interscience.
3. Ott, H. W. (1988). Noise reduction techniques in electronic systems (2nd ed.). John Wiley & Sons.
4. Keiser, B. (1989). Principles of electromagnetic compatibility (3rd ed.). Artech House.
5. Kodali, V. P. (2001). Engineering electromagnetic compatibility: Principles, measurements, and technologies with computer models (2nd ed.). IEEE Press.

E-Resources:

1. http:// www.ewh.ieee.org/soc/emcs/.
2. https://archive.nptel.ac.in/courses/108/106/108106138/.
3. https://nptel.ac.in/courses/108106138.
4. https://onlinecourses.nptel.ac.in/noc24_ee67/preview.

26AE005T	Advanced Microprocessor and Microcontroller Architectures	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand the fundamentals of microprocessor architecture.
- To study high-performance features of CISC architecture.
- To analyze high-performance features of RISC architecture.
- To learn the architecture and features of Motorola microcontrollers.
- To understand the basics of PIC microcontrollers.

Microprocessor Architecture

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

32-Bit Microprocessors

Intel 80386 Microprocessor: Architecture - Registers – Descriptors - Real Mode - Protected mode - Virtual 8086 mode - Paging and Segmentation - Comparison with 80486 Microprocessor. Pentium class of processors: RISC and CISC architectures - Superscalar Architecture - MMX technology – SSE – Pipelining - Branch Prediction techniques – FPU - Comparative study of features of Pentium-II, Pentium-III and Pentium-IV processors.

64 -Bit Microprocessors

Intel 64-bit processors: Overview of 64-bit processor execution environment – Memory organization – IA-32 memory models – Memory organization in 64-bit mode – Extended physical addressing in protected mode - Basic program execution registers – Operand addressing. Multicore Architectures: Concepts – Power reduction techniques in processors – Comparison of Intel Skylake, Goldmont and Ice Lake microarchitectures.

High-Performance RISC Architecture

Cortex-M Architecture: Introduction to Cortex-M Microcontroller, Microprocessor Architecture, Nested Interrupt Vector Controller, Bus System and Bus Matrix, Memory and Peripherals, Debug Systems, Exceptions and Interrupts Architecture, The ARM64 CPU Architecture, ARM CPU Registers The Memory Subsystem, ARM- 16/32 bit THUMB instruction set.

PIC Microcontrollers

The PIC32: Pins, Peripherals, and Special Function Registers, PIC32, The Physical Memory Map, Virtual Memory Map, Configuration Bits, Interrupts, Digital I/O, Counter/Timers, I2C Interfacing – UART, SPI, Flash memory. Activity: Write a summary of architectural features of Microprocessors designed and developed in India such as VEGA Microprocessors.

Total periods: 45

Reference Books:

1. Breg, B. B. (2008). The Intel microprocessors: Architecture, programming and interfacing. PHI.
2. Tahir, M., & Javed, K. (2017). ARM® microprocessor systems: Cortex®-M architecture, programming, and interfacing. CRC Press.

3. Lynch, K. M., Marchuk, N., & Elwin, M. L. (2015). Embedded computing and mechatronics with the PIC32 microcontroller, Newnes, Elsevier.
4. Hyde, R. (2025). The art of ARM assembly, Volume 1: 64-bit ARM machine organization and programming. No Starch Press.
5. Tabak, D. (2011). Advanced microprocessors (2nd ed.). McGraw Hill.
6. Furber, S. (2014). ARM system-on-chip architecture. Addison Wesley.
7. Miller, G. H. (2003). Micro computer engineering. Pearson Education.
8. Intel. (n.d.). Intel® 64 and IA-32 architectures software developer's manual: Vol. 1. Intel Corporation. https://www.intel.com.
9. MIT OpenCourseWare. (n.d.). OpenCourseWare. https://www.ocw.mit.edu.
10. ARM. (n.d.). ARM official website. https://www.arm.com.

26AE006T	Advanced Computer Architecture Design	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand the concepts of parallelism, partitioning, and scheduling.
- To study hardware technologies for parallel computing.
- To analyze scalable computer architectures.
- To understand vector processing principles.
- To study SIMD computer organization.

Theory of Parallelism

Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.

Partitioning and Scheduling

Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance - performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

Hardware Technologies

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory – Bus Arbitration, cache memory organisations, shared memory organisations, sequential and weak consistency models.

Pipelining, Superscalar, Parallel and Scalable Architecture

Linear and Non-Linear Pipeline processor – Instruction and Arithmetic Pipeline Design – Superscalar and Superpipeline Design – Multiprocessor Interconnects – Cache Coherence and Synchronization mechanism – Message Passing Mechanism – Flow Control Strategies – Multicast Routing Strategies.

Multivector and SIMD Computers

Vector processing Principles – Compound Vector Processing – SIMD Computer Organisation – Synchronized MIMD machine – Latency Hiding Technique – Multithreading –Scalable and Multithreaded Architectures – Data Flow and Hybrid Architectures - Parallel models, Languages and compilers, Parallel program development and environments.

Total periods: 45

Reference Books:

1. Hwang, K. (2003). Advanced computer architecture. McGraw Hill International.
2. Sima, D., Fountain, T., & Kacsuk, P. (2003). Advanced computer architecture: A design space approach. Pearson Education.
3. Shen, J. P. (2003). Modern processor design: Fundamentals of superscalar processors. Tata McGraw Hill.
4. Hwang, K. (1998). Scalable parallel computing. Tata McGraw Hill.
5. Stallings, W. (2013). Computer organization and architecture (9th ed.). Macmillan

Publishing Company.
6. Quinn, M. J. (1994). Designing efficient algorithms for parallel computers. McGraw Hill International.
7. Wilkinson, B., & Allen, M. (2005). Parallel programming (2nd ed.). Pearson Education Asia.
8. Jordan, H. F., & Alaghband, G. (2003). Fundamentals of parallel processing. Pearson Education.
9. Kain, R. Y. (2003). Advanced computer architecture: A systems design approach. PHI.
10. https://onlinecourses.nptel.ac.in/noc22_cs10/preview.

26AE007T	Signal Integrity for High-Speed Design	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand the fundamentals of signal integrity in high-speed digital systems.
- To study transmission line behaviour and impedance control.
- To analyze reflections, crosstalk, and signal degradation effects.
- To understand differential signaling and clock distribution techniques.
- To apply modeling and mitigation techniques for reliable high-speed system design.

Introduction

Introduction to Signal Integrity, Signal Quality on a Single Net, Cross Talk, Rail-Collapse Noise, Electromagnetic Interference (EMI), Signal-Integrity Solutions in Terms of Impedance: Impedance of ideal resistor, capacitor and inductor in time domain, Impedance in the Frequency Domain, Bulk Resistivity, Resistance per Length, Sheet Resistance, Power and Ground Planes and Decoupling Capacitance, Capacitance per Length, Self-Inductance and Mutual Inductance, Partial Inductance Effective, Total, or Net Inductance and Ground Bounce, Loop Self- and Mutual Inductance, Loop Inductance per Square of Planes, Loop Inductance of Planes and Via Contacts.

Activities:

1. Simulation Assignment: Use EDA tools like LTspice to simulate impedance mismatch and analyze signal degradation on a PCB trace.
2. Poster Presentation: Students prepare a poster explaining impedance behavior in the time vs frequency domain, and the concept of ground bounce and EMI.

Transmission Lines and Reflections

Speed of a Signal in a Transmission Line, Instantaneous Impedance of a Transmission Line, Characteristic Impedance and Controlled Impedance, Return Paths , Frequency Variation of the Characteristic Impedance, Reflections, Reflections from Resistive Loads, Source Impedance, Bounce Diagrams, Reflections from Short Series andShort Stub Transmission Lines, Reflections from Capacitive End Terminations, Reflections from Capacitive Loads in the Middle of a Trace, Capacitive Delay Adders, Effects of Corners and Vias, Loaded Lines, Reflections from Inductive Discontinuities, Compensation, Losses in Transmission Lines, Sources of Loss: Conductor Resistance and Skin Depth, The Dielectric, Dissipation Factor.

Activity:

3. Flipped Classroom: Students review pre-recorded videos on reflection and impedance mismatch; classroom used for solving bounce diagram exercises.
4. Hands-on Lab: Build and measure signal reflection and delay using a coaxial cable, function generator, and oscilloscope (or simulation-based equivalent).

Crosstalk

Coupling: Capacitance and Inductance, Cross Talk in Transmission Lines, Cross Talk in Uniform Transmission Lines and Saturation Length, Capacitively Coupled Currents, Inductively Coupled Currents, Near-End Cross Talk, Far-End Cross Talk, Decreasing Far-End Cross Talk, Guard Traces, Cross Talk and Dielectric, Cross Talk and Timing, Switching Noise.

Activity:

5. Case Study Analysis: Analyze real PCB designs or documented failures where crosstalk affected system reliability (e.g., DDR memory buses, HDMI lines).
6. Mini Quiz / Diagram Exercise: Conduct a quick in-class quiz identifying near-end and far-end crosstalk with diagram-based questions.

Differential Signaling

Differential Signaling, A Differential Pair, Differential Impedance with No Coupling, The Impact from Coupling, Calculating Differential Impedance, The Return-Current Distribution in a Differential Pair, Ideal Coupled Transmission-Line Model or an Ideal Differential Pair, Cross Talk in Differential Pairs, Crossing a Gap in the Return Path.

Activity:

7. Simulation/Modeling Task: Use EDA tools to model differential pairs and evaluate the effects of spacing and return path discontinuities.
8. Group Presentation: Students present on how differential signaling improves noise immunity and is used in USB, PCIe, or HDMI.

Clock Distribution and Clock Oscillators

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

Activity:

9. Timing Budgeting Exercise: Given a real-world high-speed system, students calculate skew, jitter, and timing margins for clock distribution.
10. Seminar / Tech Talk: Students present on advanced clocking techniques (e.g., PLLs, low-jitter buffers) and common clock distribution topologies.

Total periods: 45

Reference Books:

1. Bogatin, E. (Year). Signal and power integrity simplified (3rd ed.). Pearson.
2. Johnson, H., & Graham, M. (Year). High speed digital design. Prentice Hall.
3. Johnson, H. (Year). High speed signal propagation. Prentice Hall.

E-Resources

1. https://www.youtube.com/watch?v=YFwHV2EMB2A.
2. https://suddendocs.samtec.com/notesandwhitepapers/samtec-signal-integrity-handbook.pdf.
3. https://www.youtube.com/watch?v=KkfKQDnWf20.
4. https://onlinecourses.nptel.ac.in/noc24_ee67/preview.

26AE008T	VLSI Interconnects	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand the design and modeling of VLSI interconnects.
- To analyze crosstalk noise and delay in signal transmission.
- To study techniques for mitigating crosstalk effects.
- To evaluate signal integrity issues in VLSI interconnects.
- To analyze failures due to electromigration in interconnection systems.

Introduction

Types of interconnects, Interconnect trends, Coupling capacitance, Inductive effects, Interconnect metrics, Signal transmission on interconnects, On-chip interconnections, Package level interconnections, Design methodologies for interconnect, Stress void and electromigration phenomenon, Interconnections for VLSI applications, Copper interconnections, Fabrication and damascene processing, Scaling of interconnects.

Interconnect Modeling

Lossless and lossy transmission line model, Optimum line model selection, Circuit models of interconnect – Ideal, Capacitive, Resistive interconnects, Resistive interconnect trees, Scaling effects on interconnect delay, Cross-capacitances and their decoupling using Miller factor, Interconnect power.

Crosstalk in Interconnects

Definition of crosstalk, Mutual inductance and mutual capacitance, Inductance and capacitance matrix, Crosstalk-induced noise, Simulation using equivalent circuit models, Minimization of crosstalk, Crosstalk-induced delay, Energy dissipation due to crosstalk, Crosstalk effects in logic VLSI circuits.

Noise Detection and Electromigration

Crosstalk avoidance, Switching noise avoidance, Noise detection problem, Crosstalk-induced spurious signal detection, IDDx test approaches to crosstalk detection, Electromigration in VLSI interconnections, Modeling due to pulsed currents, Electromigration in copper interconnections, Failure analysis of VLSI components, Computer-aided failure analysis.

Future Interconnects

Demands in future interconnects, Optical and superconducting interconnects, Silicon nanowires and metallic interconnections, Carbon nanotube interconnections, Quantum-cell-based wireless interconnections.

Activities:

1. Design and simulate any two Circuit Models of Interconnect and observe their delay and power using EDA tools.
2. Simulate crosstalk using equivalent circuit models using EDA tools.
3. Read a recent research article on Future Interconnects and summarize the same and submit as a report.

Total periods: 45

Reference Books:

1. Goel, A. K. (2007). High-speed VLSI interconnections (2nd ed.). IEEE-Wiley.
2. Moll, F., & Roca, M. (2004). Interconnection noise in VLSI circuits. Kluwer Academic Publishers.
3. Celik, M., Pileggi, L., & Odabasioglu, A. (2002). IC interconnect analysis. Kluwer Academic Publishers.
4. Moiseev, K., Kolodny, A., & Wimer, S. (2015). Multi-net optimization of VLSI interconnect. Springer.
5. Hall, S. H., Hall, G. W., & McCall, J. A. (2000). High-speed digital system design: A handbook of interconnect theory and design practices. Wiley.
6. Saini, S. (2015). Low power interconnect design. Springer.
7. Kaushik, B. K., & Majumder, M. K. (2015). Carbon nanotube based VLSI interconnects: Analysis and design. Springer.

26AE009T	Semiconductor Memory Design	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand semiconductor memory technologies and their architectures.
- To study the operation of volatile and non-volatile memory systems.
- To analyze testing methodologies for memory devices.
- To evaluate reliability and failure mechanisms in memory systems.
- To understand memory packaging techniques and integration in electronic systems.

Random Access Memory Technologies

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation - Silicon on Insulator (SOI) Technology- SRAM Architectures and Technologies-Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures – SoftError Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

Activity:

1. Simulation Lab: Simulate SRAM and DRAM cell structures using LTspice or Cadence; analyze read/write cycles and power consumption.
2. Poster Presentation: Design posters comparing SRAM vs DRAM architectures, technologies, and applications (e.g., cache vs main memory).

Non-volatile Memories

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-GateEPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology and Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture. EEPROM on microcontroller kits (Arduino/8051) using write-read verification codes.

Activity:

1. Seminar / Presentation: Students give short talks on Flash, EEPROM, OTP, or EPROM structures and their role in real-world embedded systems.
2. Flipped Classroom: Assign students to study Flash memory architecture beforehand and solve design trade-off problems during class.

Memory Fault Modeling, Testing

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing- Application Specific Memory Testing.

Activity:

1. Quiz / Fault Identification Task: Conduct a quiz or task where students identify and classify memory fault types and appropriate test methods.
2. Testing Demo / Lab Assignment: Test RAM or EEPROM on microcontroller kits (Arduino/8051) using write-read verification codes.

Reliability and Radiation Effects

General Reliability Issues-RAM Failure Modes and Mechanism-Design for Reliability- Reliability Test Structures-Radiation Effects-Single Event Phenomenon (SEP) Radiation Hardening Techniques- Radiation Hardening Process and Design Issues Radiation Hardened Memory Characteristics.

Activity:

1. Case Study Presentation: Analyze real-world memory failures due to soft errors or radiation (e.g., aerospace) and present mitigation methods.
2. Poster / Report on Radiation Hardening: Prepare a technical poster/report on radiation effects and hardening techniques used in memory design.

Advance D Memories and Packaging Technologies

Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide(GaAs)FRAMs Analog Memories – Magnetoresistive. Random Access Memories (MRAMs) Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues- Memory Cards-High Density Memory Packaging Future Directions.

Activity:

1. Mini Project: Design a conceptual hybrid memory module (e.g., MRAM + Flash) or stacked memory using 2D/3D MCM principles.
2. Model Making / CAD Visualization: Build physical or software models of memory stacks or advanced memory cell structures using tools like Tinker CAD or Fusion360.

Total periods: 45

Reference Books:

1. Sharma, A. K. (1997). Semiconductor memories: Technology, testing and reliability. Prentice-Hall of India Private Limited.
2. Haraszti, T. P. (2001). CMOS memory circuits. Kluwer Academic Publishers.
3. Prince, B. (2002). Emerging memories: Technologies and trends. Kluwer Academic Publishers.

E-Resources

1. https://archive.nptel.ac.in/courses/117/101/117101058/.
2. https://onlinecourses.nptel.ac.in/noc21_cs47/preview.
3. https://archive.nptel.ac.in/courses/113/105/113105099/.

26AE010T	Algorithms for VLSI Physical Design Automation	Category	L	T	P	C
		PE	3	0	0	3

Course Objectives:

- To understand the fundamentals of the VLSI physical design cycle.
- To study different stages involved in physical design automation.
- To analyze algorithms used in placement, routing, and floorplanning.
- To evaluate design constraints and optimization techniques.
- To apply physical design methodologies in VLSI system implementation.

Introduction

Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles –Review of VLSI Design Automation Tools.

Data Structures and Basic Algorithms

Basic Data Structures, Graph Algorithms: Graph Search Algorithms, Spanning Tree Algorithms, Shortest Path Algorithms, Classes of Graphs in Physical Design, Relationship Between Graph Classes, Graph Problems in Physical Design, Algorithms for Interval Graphs, Algorithms for Permutation Graphs, Algorithms for Circle Graphs.

Algorithms for Layout Compaction, Placement and Partitioning

Layout Compaction: Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint Graph Compaction – Placement and Partitioning: Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithms, Partitioning: The Kernighan-Lin Partitioning Algorithm.

Algorithms for Floorplanning and routing

Floor planning: Floorplanning Concepts, Terminology and Floorplan Representation, Optimization Problems in Floorplanning, Shape Functions and Floorplan Sizing. Routing: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing.

Modelling and Simulation and Synthesis

Simulation: Gate Level Modeling and Simulation, Switch-level Modeling and Simulation – Logic Synthesis and Verification: Combinational Logic Synthesis, Binary Decision Diagrams, Two-level Logic Synthesis, High level Synthesis.

Activities:

1. Simulate the complete VLSI physical design cycle for a simple circuit using suitable CAD tools.
2. Demonstrate Binary Decision Diagram for a chosen logic function with hand calculation.
3. Demonstrate various types of delay modeling at gate level with HDL.

Total periods: 45

Reference Books:

1. Sherwani, N. A. (2017). Algorithms for VLSI physical design automation (3rd ed.). Springer.

2. Gerez, S. H. (2017). Algorithms for VLSI design automation (2nd ed.). Wiley India.
3. Alpert, C. J., Mehta, D. P., & Sapatnekar, S. S. (n.d.). Handbook of algorithms for physical design automation (1st ed.). CRC Press.

26AE011T	Statistical Analysis and Optimization for VLSI	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand sources of variations in VLSI design.
- To study statistical modeling techniques for VLSI systems.
- To analyze statistical timing and power variations.
- To evaluate yield analysis and optimization techniques.
- To apply statistical methods for reliable VLSI design.

Introduction

Sources of Variations: Process, Environmental, Modeling and other Sources of Variations, Components of Variation: Inter-die Variations, Intra-die variations, Impact on Performance.

Statistical Models and Techniques

Monte Carlo Techniques: Sampling Probability Distributions using Acceptance Rejection Method and Multivariate Gaussian random variables, Process Variation Modeling: Pelgrom's Model, Principal Components Based Modeling, Quad-Tree Based Modeling, Electromigration Modeling, Performance Modeling: Response Surface Methodology, Delay Modeling, Interconnect Delay Models: Statistical Delay Metrics.

Statistical Timing Analysis

Introduction, Block-Based Timing Analysis, Discretized Delay PDFs, Reconvergent Fanouts, Canonical Delay PDFs, Multiple Input Switching, Path-Based Timing Analysis, Parameter-Space Techniques, Bayesian Networks.

Statistical Power and Yield Analysis

Power Analysis: Leakage Models, High-Level Statistical Analysis, Gate-Level Statistical Analysis, Dynamic Power, Leakage Power: Estimating Parameters of the Distribution, Estimating the probability density function, Temperature and Power Supply Variations, Yield Analysis: High-Level Yield Estimation, Gate-Level Yield Estimation: Timing Analysis, Leakage Power Analysis, Yield Estimation, Supply Voltage Sensitivity.

Statistical Optimization Techniques

Optimization of Process Parameters, Gate Sizing, Buffer Insertion, Threshold Voltage Assignment.

Activities:

1. Perform process, voltage and temperature variation analysis using Monte-Carlo method and plot the probability density function for each parameter. (Use appropriate EDA tool).
2. Apply Bayesian Network for timing analysis for any benchmark circuit and estimate delay with hand calculations.

Total periods: 45

Reference Books:

1. Srivastava, A., Sylvester, D., & Blaauw, D. (2005). Statistical analysis and optimization for VLSI: Timing and power. Springer.
2. Shen, R., Tan, S. X.-D., & Yu, H. (2012), Statistical performance analysis and modeling techniques for nanometer VLSI designs, Springer.

26AE012T	System on Chip Design	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand SoC architecture and design methodologies.
- To study embedded processor selection and integration.
- To analyze memory design and interconnect structures in SoC.
- To explore FPGA-based SoC implementation techniques.
- To optimize area, power, and performance in SoC design.

System Architecture: Overview

Components of the system – Processor architectures – Memory and addressing – System-level interconnection – SoC design requirements and specifications – Design integration – Design complexity – Cycle time, die area and cost – Ideal and practical scaling – Area-time-power tradeoff in processor design – Configurability.

Activity: Seminar, Quiz, Flipped classroom.

Processor Selection for SOC

Overview – Soft processors, processor core selection – Instruction set, branches, interrupts and exceptions – Basic elements in instruction handling – Minimizing pipeline delays – Reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors.

Activity: Seminar, Quiz, Flipped classroom.

Memory Design

SoC external memory, SoC internal memory – Scratchpads and cache memory – Cache organization and write policies – Line replacement strategies – Split I/D-caches – Multilevel caches – SoC memory systems – Board-based memory systems – Processor/memory interaction.

Activity: Collaborative Learning.

Interconnect Architectures and SOC Customization

Bus architectures – SoC standard buses (AMBA, Core Connect) – Processor customization approaches – Reconfigurable technologies – Mapping designs onto reconfigurable devices – FPGA-based design – Architecture of FPGA – FPGA interconnect technology – FPGA memory – Floor planning and routing.

Activity: Project-Based Learning.

FPGA-Based Embedded Processor

Hardware/software task partitioning – FPGA fabric-immersed processors – Soft processors and hard processors – Tool flow for hardware/software co-design – Interfacing processor with memory and peripherals – On-chip interfaces: Wishbone, Avalon, OPB – Customized microcontroller design – FPGA-based signal interfacing and conditioning.

Activity: Industry / Field Visits.

Total periods: 45

Reference Books:

1. Flynn, M. J., & Luk, W. (2011). Computer system design: System-on-chip. Wiley India.
2. Furber, S. (2000). ARM system-on-chip architecture (2nd ed.). Addison-Wesley.
3. Vahid, F. (2001). Embedded system design: A unified hardware/software introduction. Wiley.
4. Patterson, D. A., & Hennessy, J. L. (2013). Computer organization and design: The hardware/software interface (5th ed.). Morgan Kaufmann.
5. Lin, Y.-L. S. (Ed.). (2007). Essential issues in SoC design. Springer.
6. Elmasry, M. I. (2002). System-on-chip for real-time applications. Springer.
7. Kamal, R. (2020). Embedded systems: Architecture, programming and design (3rd ed.). McGraw Hill.
8. Kaeslin, H. (2008). Digital integrated circuit design: From VLSI architectures to CMOS fabrication. Cambridge University Press.
9. Wolf, W. (2009). Modern VLSI design: IP-based design (4th ed.). Pearson Education.

E-Learning Resources:

1. NPTEL Course on "System on Chip Design" by Prof. S. Kamakoti, IIT Madras – https://nptel.ac.in.
2. Coursera – SoC Design Lab and FPGA-based Embedded Systems by University of Colorado Boulder.
3. edX – Computer Architecture and Design by MITx.
4. ARM Developer Resources – https://developer.arm.com.
5. Xilinx/Vivado Tutorials and Docs – https://www.xilinx.com.
6. Intel FPGA Training – https://www.intel.com/fpga.

26AE013T	Hardware / Software Co-Design	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand system specification and modeling techniques.
- To study partitioning strategies in system design.
- To analyze hardware and software partitioning approaches.
- To learn prototyping and emulation techniques.
- To understand verification methodologies in system design.

System Specification and Modelling

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification And Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor Architectures With One ASIC, Single-Processor Architectures With Many ASICs, Multi-Processor Architectures, Comparison of Co Design Approaches, Models of Computation, Requirements for Embedded System Specification.

Hardware/Software Partitioning

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms.

Hardware/Software Co-Synthesis

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis – Hardware/software co-synthesis algorithms: hardware – software partitioning, distributed system co-synthesis.

Prototyping and Emulation

Introduction, Prototyping And Emulation Techniques, Prototyping and Emulation Environments, Future Developments In Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.

Design Specification and Verification

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design: System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co Simulation.

Total periods: 45

Reference Books:

1. Schaumont, P. (2010). A practical introduction to hardware/software codesign. Springer.
2. Niemann, R. (1998). Hardware/software co-design for data flow dominated embedded systems. Kluwer Academic Publishers.
3. Staunstrup, J., & Wolf, W. (1997). Hardware/software co-design: Principles and practice. Kluwer Academic Publishers.

26AE014T	MEMS and NEMS	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand MEMS fundamentals and fabrication processes.
- To impart knowledge of the photolithographic process, photo resist and pattern transfer.
- To provide a fundamental of NEMS and its fabrication methods.
- To explore carbon-based NEMS materials and fabrication challenges.
- To learn about the diverse applications of MEMS and NEMS.

Fundamentals of MEMS

Introduction - Low Cost - Redundancy and Disposability – Scaling – Made – Substrates – Processing – Mask – Developing – Etching - Road Map and Perspective Silicon Substrate – Silicon Growth – Crystal - Miller Indices – Semiconductor – Doping - Additive Techniques.

Activity:

1. Case Study: Analyze the evolution and cost benefits of MEMS in healthcare diagnostics.
2. Hands-on: Silicon wafer orientation and doping simulation using open tools (e.g., NanoHUB).

Pattern Transformation of Mems

Photolithographic Process – Clean room - Photo Resist - Positive Resist - Negative Resist – Working with Resist – Applying Photo Resist - Exposure and Pattern Transfer - Printing Methods – Contact Proximity – Projection Printing - Development and Post Treatment -Masks – Resolution – Sensitivity and Resist Profiles – Mask Alignment - Permanent Resists.

Activity:

1. Lab Demo / Video Simulation: Lithography and mask alignment procedure.
2. Assignment: Design a basic mask layout for a MEMS pattern.

Introduction of NEMS

Introduction – Basic properties - Benefits of Nanomachines – Miniaturization - NEMS Memory – Importance of AFM - Top-Down Approach - NEMS devices - NEMS Advantages.

Activity:

1. Seminar: Benefits and miniaturization challenges in NEMS.
2. Simulation: NEMS memory modeling using nano-electronics simulator (NanoHub toolkit).

NEMS Materials and Fabrication

Materials – Carbon Allotropes - Carbon Based Materials - Metallic Carbon Nanotubes Difficulties – Simulations - Current Challenges and future of NEMS – Deposition processes – Lithography – Etching processes.

Activity:

1. Group Project: Design and simulate a carbon nanotube-based NEMS device.
2. Quiz: On lithography types and carbon-based nanomaterials.

Power Amplifiers

Pressure sensor - Piezoresistive sensor - Capacitive sensor – RF applications Gyroscope – Optical MEMS - Optical Data - Switching - RF MEMS - MEMS switches - MEMS Resonators. Case

study: Cantilever piezoelectric actuator, Capacitive accelerometer, Piezo resistive pressure sensor.

Activity:

1. Case Study Presentation: Comparison of MEMS gyroscope and accelerometer.
2. Assignment: Technical report on emerging RF MEMS switches.

Total periods: 45

Reference Books:

1. Stephen D. Senturia, *Microsystem Design*, Springer, 2001.
2. Marc J. Madou, *Fundamentals of Microfabrication and Nanotechnology*, CRC Press, 2011.
3. Tai-Ran Hsu, *MEMS and Microsystems: Design and Manufacture*, McGraw-Hill, 2008.
4. Julian W. Gardner, Vijay K. Varadan, and Osama O. Awadelkarim, *Microsensors, MEMS and Smart Devices*, Wiley, 2001.
5. Sergey Edward Lyshevski, *MEMS and NEMS: Systems, Devices, and Structures*, CRC Press, 2002.
6. Bharat Bhushan, *Springer Handbook of Nanotechnology*, Springer, 2017.

E-Learning Resources:

1. NPTEL – MEMS and Microsystems.
2. NanoHUB – Simulation tools for MEMS/NEMS.
3. MIT OpenCourseWare – Microsystems Technology.

26AE015T	Cryptography and Network Security	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand the fundamentals of communication networks and information security.
- To identify various types of security attacks and threats.
- To study security techniques and cryptographic algorithms.
- To ensure data integrity, confidentiality, and authentication.
- To design and implement security mechanisms in wired and wireless networks.

Introduction on Security

Security Goals, Cryptographic attacks, Security services and mechanisms Techniques: Cryptography and Steganography, Traditional Symmetric Key Ciphers: Substitution Ciphers and Transposition Ciphers, Mathematics for Cryptography.

Symmetric & Asymmetric Key Algorithms

Introduction to Block Ciphers and Stream Ciphers, Data Encryption Standards (DES), Advanced Encryption Standard (AES), RC4, Principle of asymmetric key algorithms, RSA Cryptosystem.

Integrity, Authentication and Key Management

Message Integrity, Hash functions: SHA 512, Whirlpool, Digital signatures: Digital signature standards. Authentication: Entity Authentication: Biometrics, Key management Techniques.

Network Security, Firewalls and Web Security

Introduction on Firewalls, Types of Firewalls, IP Security, E-mail security: PGP- S/MIME, Web security: SSL-TLS, SET.

Wireless Network Security

Security Attack issues specific to Wireless systems: Worm hole, Tunneling, DoS. Security for WLAN, Security for Broadband networks: Security challenges in 4G and 5G deployments, Introduction to side channel attacks and their counter measures.

Total periods: 45

Reference Books:

1. Behrouz A. Forouzan , “Cryptography and Network security”, McGraw- Hill, 2011.
2. William Stallings, "Cryptography and Network security: principles and practice", Prentice Hall of India, New Delhi, 2nd Edition,2002.
3. AtulKahate ,“Cryptography and Network security”, Tata McGraw-Hill,2nd Edition, 2008.
4. R.K.Nichols and P.C. Lekkas ,“Wireless Security: Models , threats and Solutions”, McGraw- Hill, 2001.
5. H. Yang et al., “Security in Mobile Ad Hoc Networks: Challenges and Solution”, IEEE Wireless Communications, Feb. 2004.
6. “Securing Ad Hoc Networks", IEEE Network Magazine, vol. 13, no. 6, pp. 24-30, December 1999.
7. "Security of Wireless Ad Hoc Networks," http://www.cs.umd.edu/~aram/wireless/ survey.pdf
8. David Boelet.al,“Securing Wireless Sensor Networks – Security Architecture”, Journal of networks , Vol.3. No. 1. pp. 65 -76, Jan 2008.
9. Perrig, A., Stankovic, J., Wagner, D., “Security in Wireless Sensor Networks”, Communications of

the ACM, 47(6), 53-57, 2004.
10. Introduction to side channel attacks – http://gauss.ececs.uc.edu/Courses/c653/lectures/SideC/intro.pdf.

26AE016T	Neuromorphic Computing	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand the biological foundations of neural computation and synaptic plasticity.
- To analyze spiking neural networks and neuromorphic models.
- To design CMOS/VLSI circuits for neuromorphic systems.
- To study neuromorphic hardware architectures such as Loihi and SpiNNaker.
- To develop low-power neuromorphic solutions for sensing and robotics applications.

Biological Inspiration and Neural Coding

Biological neurons and synapses: structure and function, Spike generation and propagation (Hodgkin-Huxley, Integrate-and-Fire models), Neural coding: rate code, temporal code, population code, Synaptic plasticity: Hebbian learning, STDP (Spike Timing-Dependent Plasticity), Functional models of neural computation.

Activity: Simulating Neural Spiking and Coding.

Spiking Neural Networks and Learning Algorithms

SNN architecture and neuron models (LIF, Izhikevich), Spike encoding and decoding techniques, Supervised and unsupervised learning: STDP, Reward-Modulated STDP, Reservoir computing and Liquid State Machines, SNN simulation frameworks: BRIAN2, NEST, PyNN.

Activity: Build and Train a Simple Spiking Neural Network Using BRIAN2.

VLSI Implementation of Neuromorphic Systems

Analog and digital circuit models of neurons and synapses, Current-mode vs. voltage mode designs, Subthreshold analog VLSI design for neuron circuits, Mixed-signal implementations and silicon neurons, Noise tolerance and power-efficiency in neuromorphic chips.

Activity: Design and Simulate a Subthreshold Analog Silicon Neuron.

Neuromorphic Hardware and Architectures

Architectures of Loihi (Intel), TrueNorth (IBM), SpiNNaker (Manchester), Memory-centric computing and synapse mapping, Memristor-based neuromorphic architectures, Emerging devices: Phase-change memory, Ferroelectric FETs, and STT-MRAM, Crossbar arrays and 3D integrated neuromorphic systems.

Activity: Compare and Analyze Modern Neuromorphic Hardware Architectures.

Applications and Trends in Neuromorphic Computing

Brain-computer interfaces (BCI), Edge computing using neuromorphic chips, Sensor fusion and neuromorphic perception (vision, auditory), Neuromorphic robotics and event-based control, Future directions: AI accelerators, quantum neuromorphic systems, ethical implications.

Activity: Design a Neuromorphic Application for Edge Intelligence.

Total periods: 45

Reference Books:

1. Gerstner, W., Kistler, W. M., Naud, R., & Paninski, L. (2014). Neuronal dynamics: From single neurons to networks and models of cognition. Cambridge University Press.

2. Chen, Y., Chen, T., & Li, L. (2023). Neuromorphic computing systems: Architectures, models and applications. Springer.
3. Mead, C. (1989). Analog VLSI and neural systems. Addison-Wesley.
4. Koch, C. (2004). Biophysics of computation: Information processing in single neurons. Oxford University Press.
5. Furber, S. (2006). Principles of asynchronous circuit design: A systems perspective. Springer.

E-Resources

1. Neuronal Dynamics by Gerstner et al. http://neuronaldynamics.epfl.ch/.
2. MIT OCW – Principles of Neuroscience https://ocw.mit.edu/courses/brain-and-cognitive-sciences/9-01-introduction-to neuroscience-fall-2007.

26AE017T	Hardware Architecture for Artificial Intelligence	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand the fundamentals of artificial intelligence hardware design.
- To study architectures for AI hardware implementation.
- To analyze parallel computing techniques for AI systems.
- To explore computation methods for efficient AI processing.
- To design optimized AI hardware for performance and scalability.

Introduction to Deep Learning

Development history, neural network models, neural network classification, neural network framework, neural network comparison, neural network layers, DNN development resources, deep learning challenges, key metrics and design objectives.

Parallel Architectures

Central Processing Unit (CPU), Graphics Processing Unit (GPU), Deep Learning Accelerator (NVDLA), Tensor Processing Unit (TPU), Catapult Fabric Accelerator, Streaming graph theory, Blaize graph streaming processor, Graphcore Intelligence Processing Unit.

Convolution and Sparsity Optimization

Deep convolutional neural network accelerator, Eyeriss accelerator, Network sparsity, Energy efficient inference engine, Cambricon-X accelerator, SCNN accelerator, SeerNet accelerator.

In-Memory and Near-Memory Computation

Neurocube architecture, Tetris accelerator, NeuroStream accelerator, DaDianNao supercomputer, Cnvlutin accelerator.

3D Neural Processing Architectures

3D integrated circuit architecture, power distribution network, 3D network bridge, power-saving techniques.

Activities:

1. Sketch the architecture of well-known DNN and analyze the parameters and number of computations in each layer.
2. Compare and contrast the key features of various parallel architectures and write a report on the same.
3. Consider a real time problem, and identify which architecture will be suitable for that problem. Justify your answer.
4. Analyze the effect of filter size on the performance of DNN.
5. Read a recent research article on hardware implementation strategies of Artificial Intelligence algorithms and summarize the same and submit as a report.

Total periods: 45

Reference Books:

1. Liu, A. C. C., & Law, O. M. K. (2021). Artificial intelligence hardware design: Challenges and solutions. IEEE–Wiley.
2. Sze, V., Chen, Y.-H., Yang, T.-J., & Emer, J. S. (2020). Efficient processing of deep neural networks. Morgan & Claypool.

3. Goodfellow, I., Bengio, Y., & Courville, A. (2016). Deep learning. MIT Press. https://www.deeplearningbook.org 4. Thakare, A. D., & Bhandari, S. U. (2023). Artificial intelligence applications and reconfigurable architectures. Wiley & Scrivener.

26AE018T	IP Core Design and Protection	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand the fundamentals of IP core design.
- To study different types and architectures of IP cores.
- To explore hardware IP protection techniques.
- To analyze IP authentication and security methods.
- To apply IP design methodologies in system integration.

IP Cores Design

Introduction: IP cores in a typical VLSI design flow, Classification of hardware IP, IP Modeling, IP Verification, IP Optimization, IP Protection, Gates as IP, Subsystems as IP, IP Components, Intellectual Property in Reuse-Based Design.

Hardware Intellectual Property Protection

Functional Obfuscation through State Transition Graph Modification, Extension of STG Modification for RTL Designs, Obfuscation through Control and Dataflow Graph (CDFG) Modification, Measure of Obfuscation Level, Design Flow, Implementation Results, Effect of Key Length.

Constraint-Based IP Protection

Solutions to SAT, FPGA Design of DES Benchmark, Graph Coloring and the CF IIR Filter Design, Constraint-Based Watermarking, Fingerprinting, Copy Detection, Challenges and the Generic Approach, Mathematical Foundations for the Constraint Based Watermarking Techniques, Optimization-Intensive Watermarking Techniques.

IP User's Right Protection

Motivation and Challenges, Fingerprinting Objectives, Constraint-Based Fingerprinting Techniques.

IP Authentication

Introduction, Pattern Matching Based Techniques, Forensic Engineering Techniques, Public Detectable Watermarking Techniques.

Activities:

1. Quiz for each module.
2. Write a report on Watermarking Techniques used in IP protection and authentication.
3. Analyze the effect of key length on hardware IP protection.

Total periods: 45

Reference Books:

1. Wolf, W. (2009). Modern VLSI design: IP-based design. Pearson Education.
2. Mohamed, K. S. (2016). IP cores design: From specifications to production. Springer.
3. Mukhopadhyay, D., & Chakraborty, R. S. (2015). Hardware security: Design, threats, and safeguards. CRC Press.
4. Qu, G., & Potkonjak, M. (2003). Intellectual property protection in VLSI designs: Theory and practice. Kluwer Academic Publishers.

26AE019T	Spintronics and Quantum Computing	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand the fundamentals of spin dynamics and spintronic effects
- To study spin-based electronic devices and their operation
- To introduce quantum computing concepts such as qubits, gates, and algorithms
- To analyze hardware implementations of quantum and spintronic systems
- To explore integration of spintronics with quantum computing platforms

Fundamentals of Spintronics

Electron spin, spin angular momentum, Pauli exclusion principle, Ferromagnetism, magnetic domains, exchange interaction, Spin injection and detection, Giant magnetoresistance (GMR), tunneling magneto resistance (TMR), Spin polarization and spin coherence.

Spin-Based Devices and Architectures

Spin valves, magnetic tunnel junctions (MTJs), Spin Field Effect Transistors (SpinFETs), Domain wall logic and racetrack memory, Spin torque oscillators, STT-MRAM, SOT devices, Fabrication challenges and materials for spintronic devices.

Introduction to Quantum Computing

Qubits: physical realization and quantum state representation, Quantum gates and circuits: single- and multi-qubit operations, Quantum superposition and entanglement, No-cloning theorem and quantum teleportation, Reversible logic and quantum circuit metrics.

Quantum Algorithms and Error Correction

Quantum parallelism and the Deutsch-Jozsa algorithm, Grover's algorithm and search speedup, Shor's algorithm for integer factorization, Quantum error correction codes (bit flip, phase flip, Shor code), Basics of quantum fault tolerance.

Hardware Realizations and Spin-Qubit Integration

Physical qubit implementations: superconducting, trapped ion, spin qubits; Semiconductor spin qubits: GaAs and Si-based platforms, NV centers in diamond and quantum dots, Integration of spintronics with quantum computing hardware, Cryogenic control and coherence time limitations.

Total periods: 45

Reference Books:

1. Bandyopadhyay, S., & Cahay, M. (2015). Introduction to spintronics (2nd ed.). CRC Press.
2. Awschalom, D. D., Loss, D., & Samarth, N. (2002). Semiconductor spintronics and quantum computation. Springer.
3. Nielsen, M. A., & Chuang, I. L. (2010). Quantum computation and quantum information. Cambridge University Press.
4. Hofmann, P. (2015). Solid state physics: An introduction. Wiley-VCH.
5. Tucci, R. R. (2022). Qiskit textbook: Learn quantum computing using Qiskit (Online ed.). IBM Quantum/Open Source.

E-Resources

1. NPTEL Course: Spintronics – Physics and Technology by Dr. A. Perumal, IIT Guwahati

https://nptel.ac.in/courses/115103039.

2. Simulator: IBM Quantum Lab (Qiskit online simulator) https://learning.quantum.ibm.com/.
3. MOOC Course: Quantum Computation (MITx) https://ocw.mit.edu/courses/6-845-quantum-complexity-theory-fall-2010/.
4. Simulation/Tool: QuTiP Quantum toolbox in Python http://qutip.org.

26AE020T	Analog and Mixed Signal VLSI Design	Category	L	T	P	C
		ES (PE)	3	0	0	3

Course Objectives:

- To understand the fundamentals of Analog IC design, MOSFET models, and device-level noise behavior.
- To analyze and design CMOS analog building blocks including amplifiers, current mirrors, references, and op-amps.
- To explore mixed-signal design concepts and implement circuits like data converters, comparators, and PLLs.

Introduction

Introduction to Analog IC Design, Design Flow of Analog ICs, MOSFET Characteristics and Parameters, MOSFET Models, MOS Diode, MOS Capacitors, MOS Switches, Noise in MOSFETs.

CMOS Amplifiers

Single stage amplifiers: CS, CG and CD stages, Small Signal Models, Input Output Impedances, and Frequency Response. Differential Amplifier, Cascode Amplifiers, Current Amplifiers.

CMOS Sub-Circuits

Current Sinks and Sources, Simple and Cascode current Mirrors, Wilson Current Mirror, and High Swing Current Mirror. Current and Voltage References, Band gap Reference.

CMOS Operational Amplifiers

Design of CMOS Op-Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Common-mode Rejection Ratio (CMRR), Power- Supply Rejection Ratio (PSRR), Cascode Op-Amps, and Characterization Techniques of OP-Amps.

Mixed Signal Design Fundamentals

Design of MOS Comparators, Data Converter Fundamentals, Digital-to-Analog Converters, Analog-to-Digital Converters, Switch Capacitor Circuits, Phase locked loops, Techniques of Analog Layout.

Total periods: 45

Reference Books:

1. Allen, P. E., & Holberg, D. R. (2004). CMOS analog circuit design. Oxford University Press.
2. Razavi, B. (2002). Design of analog CMOS integrated circuits. Tata McGraw-Hill.
3. Baker, R. J., Li, H. W., & Boyce, D. E. (2002). CMOS circuit design, layout, and simulation. PHI.
4. Van de Plassche, R. J. (2003). CMOS integrated analog-to-digital and digital-to analog converters. Springer.

Open Electives

26AE901T	Electric Vehicle Technology	Category	L	T	P	C
		OE	3	0	0	3

Course Objectives:

- To understand the need, evolution, and impact of electric and hybrid vehicles
- To study electric vehicle architectures and hybrid drive train configurations
- To analyze energy storage systems including batteries, ultracapacitors, and fuel cells
- To understand electric drives, motor control, and power electronics in EVs
- To design and evaluate electric vehicles based on performance, efficiency, and safety

Need For Electric Vehicles

History and need for electric and hybrid vehicles, social and environmental importance of hybrid and electric vehicles, impact of modern drive-trains on energy supplies, comparison of diesel, petrol, electric and hybrid vehicles, limitations, technical challenges.

Electric Vehicle Architecture

Electric vehicle types, layout and power delivery, performance – traction motor characteristics, tractive effort, transmission requirements, vehicle performance, energy consumption, Concepts of hybrid electric drive train, architecture of series and parallel hybrid electric drive train, merits and demerits, mild and full hybrids, plug-in hybrid electric vehicles and range extended hybrid electric vehicles, Fuel cell vehicles.

Energy Storage

Batteries – types – lead acid batteries, nickel based batteries, and lithium based batteries, electrochemical reactions, thermodynamic voltage, specific energy, specific power, energy efficiency, Battery modeling and equivalent circuit, battery charging and types, battery cooling, Ultra-capacitors, Flywheel technology, Hydrogen fuel cell, Thermal Management of the PEM fuel cell.

Electric Drives and Control

Types of electric motors – working principle of AC and DC motors, advantages and limitations, DC motor drives and control, Induction motor drives and control, PMSM and brushless DC motor drives and control , AC and Switch reluctance motor drives and control – Drive system efficiency – Inverters – DC and AC motor speed controllers.

Design of Electric Vehicles

Materials and types of production, Chassis skate board design, motor sizing, power pack sizing, component matching, Ideal gear box – Gear ratio, torque–speed characteristics, Dynamic equation of vehicle motion, Maximum tractive effort – Power train tractive effort Acceleration performance, rated vehicle velocity – maximum gradability, Brake performance, Electronic control system, safety and challenges in electric vehicles. Case study of Nissan leaf, Toyota Prius, tesla model 3, and Renault Zoe cars.

Total periods: 45

Reference Books:

1. Iqbal Hussein, Electric and Hybrid Vehicles: Design Fundamentals, 2nd edition CRC Press, 2011.
2. Mehrdad Ehsani, Yimi Gao, Sebastian E. Gay, Ali Emadi, Modern Electric, Hybrid Electric

and Fuel Cell Vehicles: Fundamentals, Theory and Design, CRC Press, 2004.
3. James Larminie, John Lowry, Electric Vehicle Technology Explained - Wiley, 2003.
4. Ehsani, M, “Modern Electric, Hybrid Electric and Fuel Cell Vehicles: Fundamentals, Theory and Design”, CRC Press, 2005.

26AE902T	Micro and Small Business Management	Category	L	T	P	C
		OE	3	0	0	3

Course Objectives:

- To understand the fundamentals and concepts of small business and entrepreneurship
- To identify and evaluate business opportunities and develop business plans
- To build managerial, leadership, and marketing skills for small business success
- To understand financial aspects including funding, working capital, and profitability
- To analyze business valuation, risk factors, and crisis management in small businesses

Introduction to Small Business

Creation, Innovation, entrepreneurship and small business - Defining Small Business –Role of Owner – Manager – government policy towards small business sector –elements of entrepreneurship –evolution of entrepreneurship –Types of Entrepreneurship – social, civic, corporate - Business life cycle - barriers and triggers to new venture creation – process to assist start ups – small business and family business.

Screening the Business Opportunity and Formulating the Business Plan

Concepts of opportunity recognition; Key factors leading to new venture failure; New venture screening process; Applying new venture screening process to the early stage small firm Role planning in small business – importance of strategy formulation – management skills for small business creation and development.

Building the Right Team and Marketing Strategy

Management and Leadership – employee assessments – Tuckman's stages of group development - The entrepreneurial process model - Delegation and team building - Comparison of HR management in small and large firms - Importance of coaching and how to apply a coaching model.

Marketing within the small business - success strategies for small business marketing - customer delight and business generating systems, - market research, - assessing market performance- sales management and strategy - the marketing mix and marketing strategy.

Financing Small Business

Main sources of entrepreneurial capital; Nature of 'bootstrap' financing - Difference between cash and profit - Nature of bank financing and equity financing - Funding-equity gap for small firms. Importance of working capital cycle - Calculation of break-even point - Power of gross profit margin- Pricing for profit - Credit policy issues and relating these to cash flow management and profitability.

Valuing Small Business and Crisis Management

Causes of small business failure - Danger signals of impending trouble - Characteristics of poorly performing firms - Turnaround strategies - Concept of business valuation - Different valuation measurements - Nature of goodwill and how to measure it - Advantages and disadvantages of buying an established small firm - Process of preparing a business for sale.

Total periods: 45

Reference Books:

1. Hankinson,A. (2000). “The key factors in the profile of small firm owner-managers that influence business performance. The South Coast Small Firms Survey, 1997-2000.” Industrial and Commercial Training 32(3):94-98.
2. Parker,R.(2000). “Small is not necessarily beautiful: An evaluation of policy support for small and medium-sized enterprise in Australia.” Australian Journal of Political Science 35(2):239 253.
3. Journal articles on SME’s.

26AE903T	Renewable Energy Technology	Category	L	T	P	C
		OE	3	0	0	3

Course Objectives:

- To understand different types of renewable energy technologies and their characteristics
- To study standalone and grid-connected renewable energy systems
- To analyze solar photovoltaic systems and their performance characteristics
- To understand wind energy conversion systems and their operation
- To explore various other renewable energy sources and their applications

Introduction

Classification of energy sources – Co2 Emission - Features of Renewable energy - Renewable energy scenario in India -Environmental aspects of electric energy conversion: impacts of renewable energy generation on environment Per Capital Consumption - CO2 Emission - importance of renewable energy sources, Potentials – Achievements– Applications.

Solar Photovoltaics

Solar Energy: Sun and Earth-Basic Characteristics of solar radiation- angle of sunrays on solar collector-Estimating Solar Radiation Empirically - Equivalent circuit of PV Cell- Photovoltaic cell characteristics: P-V and I-V curve of cell-Impact of Temperature and Insolation on I-V characteristics-Shading Impacts on I-V characteristics-Bypass diode -Blocking diode.

Photovoltaic System Design

Block diagram of solar photo voltaic system : Line commutated converters (inversion mode) - Boost and buck-boost converters - selection of inverter, battery sizing, array sizing - PV systems classification- standalone PV systems - Grid tied and grid interactive inverters- grid connection issues.

Wind Energy Conversion Systems

Origin of Winds: Global and Local Winds- Aerodynamics of Wind turbine-Derivation of Betz's limit- Power available in wind-Classification of wind turbine: Horizontal Axis wind turbine and Vertical axis wind turbine- Aerodynamic Efficiency-Tip Speed-Tip Speed Ratio-Solidity-Blade Count-Power curve of wind turbine - Configurations of wind energy conversion systems: Type A, Type B, Type C and Type D Configurations- Grid connection Issues - Grid integrated SCIG and PMSG based WECS.

Other Renewable Energy Sources

Qualitative study of different renewable energy resources: ocean, Biomass, Hydrogen energy systems, Fuel cells, Ocean Thermal Energy Conversion (OTEC), Tidal and wave energy, Geothermal Energy Resources.

Total periods: 45

Reference Books:

1. S.N.Bhadra, D. Kastha, & S. Banerjee "Wind Electrical Systems", Oxford University Press.
2. Rai. G.D, "Non conventional energy sources", Khanna publishes, 1993. Rai. G.D," Solar energy utilization", Khanna publishes, 1993.
3. Chetan Singh Solanki, "Solar Photovoltaics: Fundamentals, Technologies and

Applications", PHI Learning Private Limited, 2012.
4. John Twideu and Tony Weir, "Renewal Energy Resources" BSP Publications, 2006
5. Gray, L. Johnson, "Wind energy system", prentice hall of India, 1995.
6. B.H.Khan, " Non-conventional Energy sources", , McGraw-hill, 2nd Edition, 2009.
7. Fang Lin Luo Hong Ye, " Renewable Energy systems", Taylor & Francis Group,2013.

26AE904T	Design Thinking and User Experience	Category	L	T	P	C
		OE	3	0	0	3

Course Objectives:

- To provide a sound knowledge in UI & UX
- To understand the need for UI and UX
- Research Methods used in Design
- Tools used in UI & UX
- Creating a wireframe and prototype

Ux Lifecycle Template

Introduction. A UX process lifecycle template. Choosing a process instance for your project. The system complexity space. Meet the user interface team. Scope of UX presence within the team. More about UX lifecycles. Business Strategy. Value Innovation. Validated User Research. Killer UX Design. The Blockbuster Value Proposition.

Contextual Inquiry

The system concept statement. User work activity data gathering. Look for emotional aspects of work practice. Abridged contextual inquiry process. Data-driven vs. model-driven inquiry. Organizing concepts: work roles and flow model. Creating and managing work activity notes. Constructing your work activity affinity diagram (WAAD). Abridged contextual analysis process. History of affinity diagrams.

Design Thinking, Ideation, and Sketching

Design-informing models: second span of the bridge . Some general “how to” suggestions. A New example domain: slideshow presentations. User models. Usage models. Work environment models. Barrier summaries. Model consolidation. Protecting your sources. Abridged methods for design-informing models extraction. Design paradigms. Design thinking. Design perspectives. User personas. Ideation. Sketching.

Ux Goals, Metrics, and Targets

Introduction. UX goals. UX target tables. Work roles, user classes, and UX goals. UX measures. Measuring instruments. UX metrics. Baseline level. Target level. Setting levels. Observed results. Practical tips and cautions for creating UX targets. How UX targets help manage the user experience engineering process.

Analysing User Experience

Sharpening Your Thinking Tools. UX Research and Strength of Evidence. Agile Personas. How to Prioritize Usability Problems. Creating Insights, Hypotheses and Testable Design Ideas. How to Manage Design Projects with User Experience Metrics. Two Measures that Will Justify Any Design Change. Evangelizing UX Research. How to Create a User Journey Map. Generating Solutions to Usability Problems. Building UX Research Into the Design Studio Methodology. Dealing with Common objections to UX Research. The User Experience Debrief Meeting. Creating a User Experience Dashboard.

Activities:

1. Hands on Design Thinking process for a product.
2. Defining the Look and Feel of any new Project.

3. Create a Sample Pattern Library for that product (Mood board, Fonts, Colors based on UI principles).
4. Identify a customer problem to solve.
5. Conduct end-to-end user research - User research, creating personas, Ideation process (User stories, Scenarios), Flow diagrams, Flow Mapping.

Total periods: 45

Reference Books:

1. UX for Developers: How to Integrate User-Centered Design Principles Into Your Day-to Day Development Work, Westley Knight. Apress, 2018.
2. The UX Book: Process and Guidelines for Ensuring a Quality User Experience, Rex Hartson, Pardha Pyla. Morgan Kaufmann, 2012 103.
3. UX Fundamentals for Non-UX Professionals: User Experience Principles for Managers, Writers, Designers, and Developers, Edward Stull. Apress, 2018.
4. Lean UX: Designing Great Products with Agile Teams, Gothelf, Jeff, Seiden, and Josh. O'Reilly Media, 2016.
5. Designing UX: Prototyping: Because Modern Design is Never Static, Ben Coleman, and Dan Goodwin. SitePoint, 2017.

Approved by
Academic Council Meeting
No.: 01 Dated: 21.4.26

Recommended by
Board of Studies of M.E (AE) Dept.
Meeting No.: 01 Dated: 28.3.26

26AE905T	New Product Development	Category	L	T	P	C
		OE	3	0	0	3

Course Objectives:

- To understand the principles of generic product development processes and organizational structure.
- To identify opportunities and plan for new product development.
- To analyze customer needs and define product specifications.
- To generate, select, and evaluate product design concepts.
- To apply industrial design principles and develop prototypes for new products.

Introduction To Product design & Development

Introduction – Characteristics of Successful Product Development – People involved in Product Design and Development – Duration and Cost of Product Development – The Challenges of Product Development – The Product Development Process – Concept Development: The Front-End Process – Adapting the Generic Product Development Process – Product Development Process Flows – Product Development Organizations.

Opportunity Identification & Product Planning

Opportunity Identification: Definition – Types of Opportunities – Tournament Structure of Opportunity Identification – Effective Opportunity Tournaments – Opportunity Identification Process – Product Planning: Four types of Product Development Projects – The Process of Product Planning.

Identifying Customer Needs & Product Specifications

Identifying Customer Needs: The Importance of Latent Needs – The Process of Identifying Customer Needs. Product Specifications: Definition – Time of Specifications Establishment - Establishing Target Specifications – Setting the Final Specifications.

Concept Generation, Selection & Testing

Concept Generation: Activity of Concept Generation – Structured Approach – Five step method of Concept Generation. Concept Selection: Methodology – Concept Screening and Concepts Scoring. Concept testing: Seven Step activities of concept testing.

Industrial Design & Prototyping

Industrial Design: Need and Impact–Industrial Design Process. Prototyping – Principles of Prototyping – Prototyping Technologies – Planning for Prototypes.

Total periods: 45

References:

1. Belz A., 36-Hour Course: "Product Development" McGraw-Hill, 2010.
2. Rosenthal S.,"Effective Product Design and Development", Business One Orwin,Homewood, 1992,ISBN1-55623-603-4.
3. Pugh.S,"Total Design Integrated Methods for Successful Product Engineering", Addison Wesley Publishing,1991,ISBN0-202-41639-5.
4. Chitale, A. K. and Gupta, R. C., Product Design and Manufacturing, PHI Learning, 2013.
5. Jamnia, A., Introduction to Product Design and Development for Engineers, CRC Press,2018.

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